Analysis of Classical Five Level Inverter Topologies with SPWM Technique

Rashmi Sharma
Electrical Engineering Department, Indus University, India

Abstract: *Multilevel inverters are emerged as a very attractive choice for various medium and high voltage industrial applications. Multilevel inverters continue to receive more and more attention because of their high voltage operation capability, low switching losses, high efficiency and low output of Electro Magnetic Interference (EMI). Several multilevel inverters topologies have been introduced like diode-clamped (neutral-clamped), capacitor-clamped (flying capacitors), and cascaded H-bridge inverter. In this paper comparison of these three c1assical topologies of multilevel inverter is presented and their performance is analyzed using MATLAB-SIMULINK software. Also special attention is given to the THD of output voltage of the multilevel inverter using SPWM techniques.*

Keywords: **Multilevel inverter(MLI), Cascaded H-Bridge(CHB) Inverter, diode-clamped (neutral-clamped), capacitor-clamped (flying capacitors) Sinusoidal pulse width modulation**

1. INTRODUCTION

Multilevel inverters continue to receive more and more attention because of their high voltage operation capability, low switching losses, high efficiency and low output of Electro Magnetic Interference (EMI). The term multilevel starts with the three-level inverter introduced by Nabae et al (1981). Nowadays, multilevel inverters are becoming increasingly popular in power applications, as multilevel inverters have the ability to meet the increasing demand of power rating and power quality associated with reduced harmonic distortion and lower electromagnetic interference

Multilevel inverters have an arrangement of power switching devices and capacitor voltage sources. These inverters are suitable for high-voltage applications because of their ability to synthesize output voltage waveforms with a better harmonic spectrum and attain higher voltages with a limited maximum device rating. MLIs are used in various medium and high voltage application such as UPS, renewable energy sources, FACTS, drives and aircraft systems, etc. [4]- [5]. Multilevel inverter consists of switches (IGBTs, MOSFETs) and voltage sources, whose output is voltage with stepped waveforms [6]. The term multilevel starts with the three level introduced in [3]- [4]. As the number of level increases output voltage has more steps, the output of inverter generate voltages with stepped waveforms results in less harmonics distortion. But at higher number of levels complexity is increases and voltage imbalance problem is introduced.

2. Multilevel Inverter Topologies

There are three different topologies of MLIs: diode clamped(neutral-clamped) inverter; capacitor clamped (flying capacitors) inverter; and cascaded-bridge

inverter [1], [3], [6]. While there are different control techniques to control these multilevel inverters such as sinusoidal PWM, space vector PWM, etc [3]. This paper present comparison of different five level multilevel inverters and their response with SPWM control techniques. And special attention is given to THD of these different techniques.

1. Diode clamped Multilevel Inverter (FC-MLI):

The diode-clamped inverter (neutral-point clamped inverter) was introduced by Nabae et al (1981). The diode-clamped inverter consists of two pairs of series switches (upper and lower) in parallel with two series capacitors where the anode of the upper diode is connected to the midpoint (neutral) of the capacitors and its cathode to the midpoint of the upper pair of switches; the cathode of the lower diode is connected to the midpoint of the capacitors and divides the main DC voltage into smaller voltages. The middle point of the two capacitors can be defined as the “neutral point”. The NPC uses a single dc bus that is subdivided into a number of voltage levels by a series string of capacitors. For a five-level diode-clamped inverter if the point O is taken as the ground reference, A d.c link is divided into four capacitors Cl, C2, C3 and C4 and connects to switches in series through c1amping diodes. Due to this arrangement one capacitor voltage will appear across each switch. If d.c. link voltage is Vdc, then voltage across each capacitor will be Vdc/4. This topology requires (n-1) x (n-2) c1amping/blocking diodes per phase, if each diode has voltage rating same as active device voltage rating. Here n is number of inverter output voltage levels. Means, requirement of c1amping diodes increases with increase in, which makes the topology bulky and impractical. In Fig. 1. power circuit of single phase five level NPC-MLI is shown

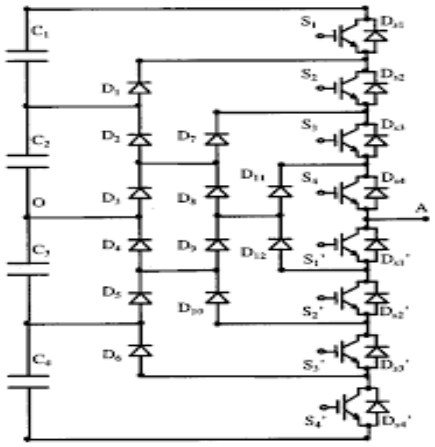

Figure. 1: Single Phase Five Level NPC-MLI

2. Capacitor-Clamped Multilevel Inverter (FC-MLI):

The capacitor-clamped multilevel inverter known as flying capacitor is similar to the diode-clamped inverter was presented in Hochgraf et al (1994) and Lai et al (1996). The capacitor-clamped multilevel inverter topology provides more

flexibility in waveform synthesis and balancing voltage. In capacitor-clamped inverter, the diode in the diode-clamped topology is replaced by clamping capacitors or floating capacitors to clamp the voltages. Each phase-leg has an identical structure. The size of the voltage increment between two capacitors determines the size of the voltage levels in the output waveform.

Capacitor-clamped multilevel inverter topologies are relatively new compared to the diode-clamped or the cascaded H-bridge cell inverter topologies. Redundancy in the switching states is available by using flying capacitors instead of clamping diodes. This redundancy can be used to regulate the capacitor voltages and obtain the same desired level of voltage at the output. Figure 2.3 shows a single-phase five-level capacitor-clamped multilevel inverter topology. The voltage across the capacitors is considered to be half of DC source voltage. For n level inverter (n-i) main capacitors and (n-1) (n-2)/2 auxiliary capacitors are required in each phase leg, if voltage rating of each capacitor is same as that of switch. Each phase leg has identical structure. This topology offers more flexibility in voltage synthesis as two or more valid switching states (redundancy) are possible. Similar to NPC-MLI this topology also requires large number of capacitors which makes it bulky and expensive.

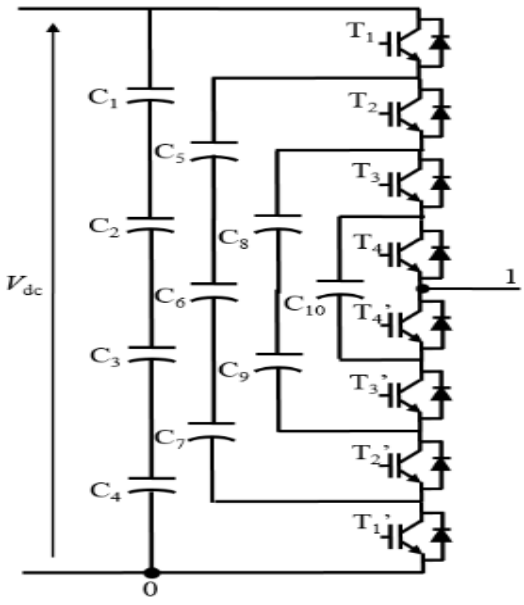

Figure. 2: Single Phase Five Level FC-MLI

3. Cascaded H Bridge Multilevel Inverter (CHB-MLI):

Cascaded H Bridge multilevel inverter is also known as multi-cell inverter. In this topology H-bridges with separate dc sources of equal magnitude are connected in series. This characteristic makes the topology modular. Total output voltage is obtained by adding voltages generated by each H-bridge.[1] Each H-bridge generates three voltage levels +Vdc, 0, -Vdc by connecting dc source to ac. output

by different combinations of the four switches used in it. For n level inverter number of cells required is(n-1)/2. This topology requires minimum number of components as there is no extra c1amping diodes and capacitors. But it requires separate D.C. source for each H-bridge [8]. Therefore, its applications are limited to areas where isolated dc sources are available. It uses two separate dc. sources and generates output Figure 3. shows single phase five level CHB-MLI. It uses two separate dc sources and generates output voltage with five levels.

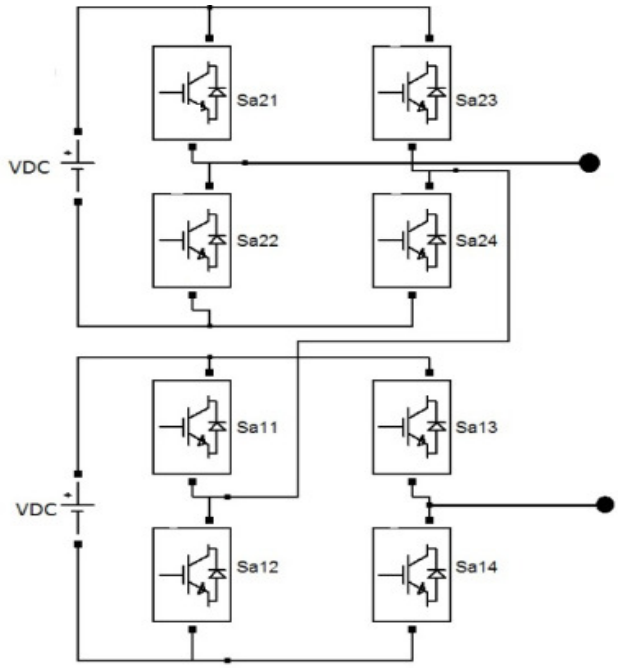

Figure. 3: Single Phase Five Level CHB-MLI

3. CONTROL AND MODULATION TECHNIQUES OF MULTILEVEL INVERTERS

Modulation techniques that work with high switching frequencies have many commutations for the power semiconductors in a cycle of the fundamental output voltage. Multilevel inverters generate sinusoidal voltages from discrete voltage levels, and Pulse Width-Modulation (PWM) strategies accomplish this task of generating sinusoids of variable voltages and frequencies[4]. Several techniques for the implementation of PWM for multilevel inverters have been developed. The well-known high switching frequency methods are classic carrier based Sinusoidal PWM (SPWM) and Space Vector PWM.

In SPWM, a sinusoidal reference wave is compared with triangular carrier waveform to generate gate pulses for switches of inverter. This traditional PWM technique can be applied to multi-level inverter topologies by using multiple carriers. Therefore, it is known as multi-carrier PWM technique. For n level inverter (n-1) carriers are required [21]. It can be further c1assified as Level Shifted PWM (LSPWM-vertical arrangement of

carrier signals) and Phase Shifted PWM (PSPWM-horizontal arrangement of carrier signals) [17], [22-24]. LSPWM leads to less distorted line voltages since all the carriers are in phase compared to PSPWM. LSPWM is further categorized as Phase Disposition-PD, Phase Opposition Disposition POD, Alternate Phase Opposition Disposition-APOD.

4. Simulation and Results

Multicarrier PD-PWM scheme is applied to all the three topologies of three phase five level inverter. Simulations are performed by using MATLAB-Simulink software. It is simulated using R-L load.

The parameters are chosen as under:

DC voltage (Vdc) = 400 V for NPC-MLI and FCMLI,

DC voltage (Vdc) = 100 V for CHB-MLI

Switching frequency (fz) = 1 kHz

Load: R=100 ohms, L=10 mH

The line voltage, FFT & THD of line voltage waveforms for inverter operation of all the topologies are presented from Fig.4 and gate pulse genration in Fig.5 For five level inverter, the number of steps x in phase voltage with respect to 0 are 4, that are Vdc/2, Vdc/4,0, -Vdc/4 and -Vdc/2. Then number of levels in line voltage m is m =2(n)+1.

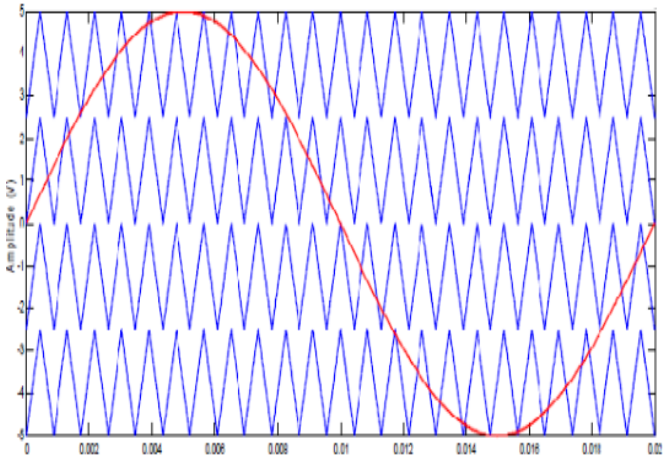

Figure 4: PD-PWM pulse generation for five level Inverter

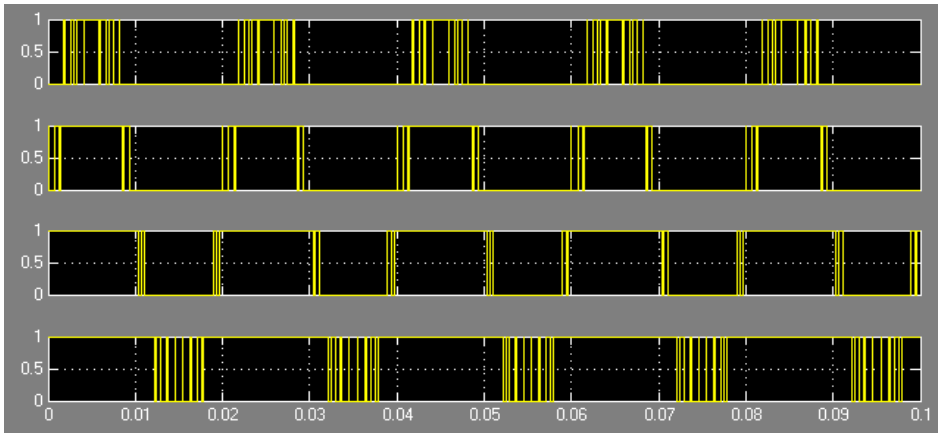

Figure5: Pulse generation for five level Inverter

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5. Comparison of All Multilevel inverter Topologies

From simulation results of all five level inverter topologies NPC-MLI, FC-MLI and CHB-MLI it can be seen that they use, eight that means same number of switches per phase. However, NPC-MLI uses twelve clamping diodes per phase and FC-MLI uses six balancing capacitors per phase. CHB-MLI uses least number of semiconductor devices. Regarding modulation all the three topologies has been investigated using multicarrier PD-PWM technique. A novel pulse generation circuit is designed. They are simulated using MA TLAB/ Simulink and the results have been analyzed to get the % THD of the output waveforms.

In order to get THD level of the waveform, a Fast Fourier Transform (FFT) is applied to obtain the spectrum of the output voltage. The % THD analysis of the line to line voltage waveforms are tabulated in the Table 1 given below. It was observed that the harmonic distortion is less in the CHB-MLI as compared to the remaining two topologies.

S. No.	Inverter Topology	Cascaded H-Bridge	Diode Clamped	Flying Capacitor
1	Main switching device	2(m-1)	2(m-1)	2(m-1)
2	Main Diodes	2(m-1)	2(m-1)	2(m-1)
3	Clamping Diodes	0	(m-1) (m-2)	0
4	DC bus capacitor	(m-1)/2	(m-1)	(m-1)
5	Balancing Capacitor	0	0	(m-1)(m-2)/2
7	DC Bus Sharing	Separate DC Source	DC Bus Sharing	DC Bus Sharing
8	THD%	47.84%	51.7%	48.4%

Table -1 Comparison of five level Inverter Topologies

6. Conclusion

This paper work includes the comparison of five level single phase multilevel inverter configurations of various types from various aspects using SPWM techniques. The study of different multilevel technique for five level inverter with PD-PWM modulation method has been done in MATLAB/SIMULINK environment. This study includes comparison of required least number of components to obtain same voltage levels and CHB-MLI is found to be appropriate among other configurations of MLI due to its modular structure, solution of voltage balancing, fault clearing ability for higher levels. Output voltage levels along with %THD has been shown and compared for five level inverter.

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