HARMONICS INVESTIGATION OF A HYBRID ACTIVE NEUTRAL POINT CLAMPED FLYING CAPACITOR FIVE LEVEL INVERTER WITH SVPWM AND SPWM

Pradeep Kumar[1], Abhijeet Patil[2]
[1]M.Tech Scholar, [2]Assistant Professor
Department of Electrical Engineering
SRK University, Bhopal, Madhya Pradesh, India
[1]pradeep459bit@gmail.com, [2]abhijeet.patil20@gmaill.com

ABSTRACT: In the field of high power and medium voltage application, the multilevel inverters seem to be the most promising alternative. The proposed a new five-level hybrid topology combining features of neutral point clamped and flying capacitor Multi-level inverters. The proposed topology provides a tradeoff between different component counts to achieve a good loss distribution, avoid direct series connection of semiconductor devices, keep the balanced operation of dc-link capacitors while keeping the number of costly components such as capacitors and switches low. The Pulse width modulation strategy for this hybrid topology has designed using modified SVPWM technique.

In SVPWM technique, the voltage reference provided using revolving reference vector. In this case magnitude and frequency of the fundamental component in line side is controlled by the magnitude and frequency respectively of the reference voltage vector. Space vector modulation techniques utilize the DC bus voltage more efficiently and generate less harmonic distortion when compared to sinusoidal PWM (SPWM) technique.

The space vector pulse width modulation control technique has been applied to five level flying capacitor inverter and their performance has been analysed by using MATLAB /Simulink. The output shows better performance results. The variations based in Total harmonics distortion are also analysed.

KEYWORDS: Neutral Point flying Clamped Inverter (NPFCI), Total Harmonic Distortion (THD), Sinusoidal Pulse Width Modulation (SPWM), Space Vector Pulse Width Modulation (SVPWM).

I. INTRODUCTION

With Power electronic converters, especially dc/ac PWM inverters have been extending their range of use in industry because they provide reduced energy consumption, better system efficiency, improved quality of product, good maintenance, and so on. For a medium voltage grid, it is troublesome to connect only one power semiconductor switches directly [1] As a result; a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations such as laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on.

As a cost effective solution, multilevel converter not only achieves high power ratings, but also enables the use of low power application in renewable energy sources such as photovoltaic, wind, and fuel cells which can be easily interfaced to a multilevel converter system for a high power application.

The inverters in such application areas as stated above should be able to handle high voltage and large power. For this reason, two-level high-voltage and large-power inverters have been designed with series connection of switching power devices such as gate-turn-off thyristors (GTOs), integrated gate commutated transistors (IGCTs), and integrated gate bipolar transistors The inverters in such application areas as stated above should be able to handle high voltage and large power.

For this reason, two-level high-voltage and large-power inverters have been designed with series connection of switching power devices such as gate-turn-off thyristors (GTOs), integrated gate commutated transistors (IGCTs), and integrated gate bipolar transistors .The inverters in such application areas as stated above should be able to handle high voltage and large power.

For this reason, two-level high-voltage and large-power inverters have been designed with series connection of switching power devices such as gate-turn-off thyristors (GTOs), integrated gate commutated transistors (IGCTs), and integrated gate bipolar transistors (IGBTs), because the series connection allows reaching much higher voltages.

However, the series connection of switching power devices has big problems [13], namely, non-equal distribution of applied device voltage across series-connected devices that may make the applied voltage of individual devices much higher than blocking voltage of the devices during transient and steady-state switching operation of devices.

Multilevel converters are a very attractive solution for medium-voltage high-power conversion applications; such as motor drives, microgrids, and distributed generation systems.

The main features of these topologies, as compared with the two-level voltage-source converters (VSC), are their capabilities to reduce:

1) Harmonic distortion of the ac-side waveforms;
2) dv/dt switching stresses;
3) Switching losses; and

Multilevel inverters have gained interest during the last three decades due to the increasing demand for medium to high voltage converters for a variety of high power applications. Different topologies have been proposed to fit the requirements of different applications.

For medium voltage inverters, cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitor (FC) are the primary topologies. Among them, NPC and FC provide a common dc-link which is a strict requirement for many applications [6].

FC inverter uses capacitors to generate output voltage levels. The availability of interphase l redundant states in this topology can provide both capacitor voltage balancing and power loss distribution among switches [7]. However, increased numbers of flying capacitors at higher levels that increases the initial cost and maintenance surcharges and decreases the reliability of the inverter along with the capacitor pre-charge in some applications are the main drawbacks of this topology [8].

NPC inverter uses diodes to clamp the voltage levels generated at the dc-link capacitors to the output. Excessive number of diodes, unbalanced operation of dc-link's voltage divider capacitors, and uneven distribution of loss among switches are major problems of this topology. Space vector algorithms are available to alleviate the unbalanced loss and capacitor voltage problems based on the inverter's operating condition [5]. Active NPC (ANPC) improves the loss distribution of NPC by replacing diodes with active switches providing alternative neutral point path [9].

Hybrid topologies are viable solutions where higher number of levels is required. Combining the advantages of CHB, FC, and NPC, hybrid inverters can provide loss and voltage balancing while keeping the number of components low. Examples of hybrid topologies combining FC and NPC can be found in [10]–[12], some of which has already found industrial applications. The 5-level FC-ANPC is an example of hybrid topologies that made its way to the industry. The ACS2000 family of medium voltage drives, commercialized by ABB, uses this topology with both active and passive front end configurations.

The main advantage of this topology is the use of a single flying capacitor to generate the output five levels. Compared to other topologies that provide a common dc-link, FC-ANPC has provided an acceptable tradeoff between the cost, performance, and reliability for 5-level applications. The disadvantages of FC-ANPC are high

number of switches, series connection of high voltage switches, and poor loss distribution [13]. The proposes a new 5-level hybrid topology based on FC and NPC inverters. The goal of the proposed topology is to overcome the shortcomings of the traditional FC-ANPC. Thus, comparatively, the proposed topology provides better loss distribution, avoids direct series connection of high voltage switches, and eliminates 2 switches per phase leg.

These advantages come at the cost of an additional capacitor and 6 diodes. Nevertheless, the lifetime of each capacitor is expected to prolong due to the half cycle operation and lower rms current.

Power electronic researchers have place in continuous efforts in developing topologies that retain the inherent edges of construction inverters with lesser range of power switches and different extra options.

With the arrival of latest topologies, a larger stress is additionally placed on to research new switching strategies. This is because of the fact that a particular switching strategy for a given topology can result in improvement of harmonic profile of output waveform as well as reduction in switching and conduction power losses. The three switching methods most discussed in the literature are:

- Carrier-based PWM
- Selective Harmonic Elimination
- Space-vector PWM
- Optimized Harmonic PWM (OHPWM)

II. Neutral Point Clamped Multi- Level Inverter

The most commonly used topology in the multilevel inverter is the diode-clamped inverter, in which the diode is used to clamp the dc voltage, to get output voltage steps. Fig. 1 shows a circuit for a three-and a four-level diode clamped inverter. Diodes D_1 and D_2 gives the main difference between the 2-level inverter and the 3- level inverter. Both devices are connected to half the voltage of the dc bus voltage.

The voltage of the N clamped inverter at steady state across each condenser is generally V_{dc} / n-1. Each active switch is required only to block V, but the clamping equipment has different ratings. The inverter with diode clamps provides multiple voltage levels by connecting the phases to a set of condensers.

The concept can be extended to a variety of different levels according to the original invention by increasing the number of condensers. This topology was first described only in three levels, where two condensers were connected across the dc bus and thereby resulted in one additional level. The other level was neutral to the dc bus so that the inverter of the neutral terminology point clamped (NPC) was introduced.

But the neutral point is not accessible with an equal number of voltage levels, and multi-pointed points (MPC) terms can sometimes be used. The diode-clamped inverter implementation was limited to three levels due to problems of voltage balancing of capacitors. The 3- level inverter is now widely used in industrial applications due to industrial developments over the past couple of years.

NPC type multilevel inverters plays crucial role in the field of power electronics and being widely used in different industrial and commercial applications because it possesses low electromagnetic interference and the effectiveness is considerably high. NPC Multilevel inverters have become more preferred over the years in electric high power application with the confirmation of less disturbances and the possibility to operate at lower switching frequencies than typical two-level inverters.

Diode-clamped topology is proposed by Nabae et al. Figure 1 shows a three level diode-camped inverter, where the DC bus voltage is divided into three levels by two bulk capacitors connected in series. The output voltage has three states: Vdc/2, 0, - Vdc/2. The diodes D_1 and D_2 provide a path for the currents at the voltage increments. Diode-clamped inverters are mostly limited to the original three-level structure due to the capacitor voltage balancing issues.

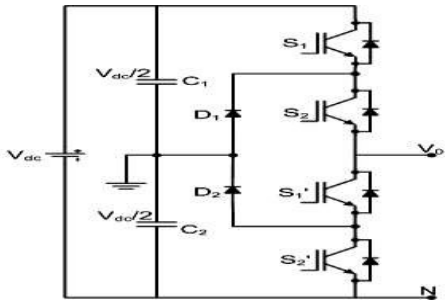

Figure 1: Neutral Point Clamped Inverter

Advantages

- The 3 phases share a standard DC-bus minimizing the capacitance needs.
- The DC-link capacitors are often pre-charged, as a group.
- High potency for fundamental shift.

Disadvantages

- Increased count of clamping diodes.
- Neutral point control for voltage balancing across the DC-link capacitors should be achieved for all conditions of operation.

III. Motivation and Problem Statement

There are many disadvantages of classical pulse generator used for generation of switching pulses. It does not give satisfactory results of harmonics. For achieving sinusoidal voltage or current signals and to reduce harmonics, multicarrier based sinusoidal PWM is the best choice to overcome the limitations of a pulse generator. For the realization of inverter in the high power applications, simple pulse generator is not effective to use, while multicarrier sinusoidal PWM strategies are more productive to use. Thus, in order to get sinusoidal, balanced and very much reduced THD, the combination of asymmetric CHB inverters with multicarrier sinusoidal PWM combination is a good approach application.

The principal disadvantage in all these variants is the large voltage requirements (IGBTs, MOSFET etc.) when increasing the number of level. Especially when it comes to three-phase inverter; the actual circuits implemented are therefore complex and costly.

An additional disadvantage is that the multi-level inverter operation requires complex control circuits. Not only is the number of gate-driven circuits high, but since the level of the DCs in all condensers must be balanced, their coordination is a complex task that a strong (and thus expensive) processor must undertake.

All in all these characteristics (comprehensive power circuits, large number of gate control and high computer loads) combine to make the multi-stage inverter a solution that can only be applied to powerful applications such as marine motors, massive chemicals and high-performance transmission systems.
The main objective of work is:

1. To develop five levels neutral point flying capacitor using space vector modulation technique.
2. To develop five levels neutral point flying capacitor using sinusoidal pulse width modulation technique.
3. Compare the result based on THD for proposed inverter system.

IV. *Multilevel Inverter*

With A dc voltage Vdc series connected capacitors constitute the energy tank for converter providing some nodes to which the multilevel converter can be connected .each capacitor to has the same voltage E_m which is given by

$$E_m = \frac{V_{dc}}{m-1} \quad (1)$$

Where, m denotes the number of levels. The level is referred to as the number of nodes to which the inverter can be accessible. An m-level inverter needs (m-1) capacitors. There are several types of multilevel converters.

The types of multilevel converters are: diode-clamped multilevel converters, flying-capacitor (also referred to as capacitor-clamped) multilevel converters, and cascaded H-bridges multilevel converters At this point, it seems appropriate to discuss the difference between the terms "multilevel converter" and "multilevel inverter."

The term "multilevel converter" refers to the converter itself. Furthermore, the connotation of the term is that power can flow in one of two directions. Power can flow from the ac side to the dc side of the multilevel converter. This method of operation is called the rectification mode of operation. Power can also flow from the dc side to the ac side of the multilevel converter.

This method of operation is called the inverting mode of operation. The term "multilevel inverter" refers to using a multilevel converter in the inverting mode of operation. The line voltage consists of a positive phase-leg *a* voltage and a negative phase-leg *b* voltage. Each phase voltage tracks one-half of the sinusoidal waves.

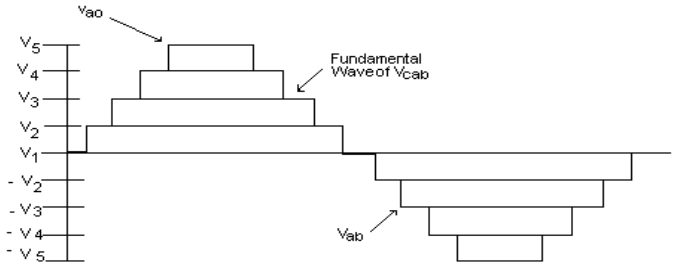

Figure 2: Source Converter

Phase and line voltage waveforms of a 5-level diode-clamp voltage

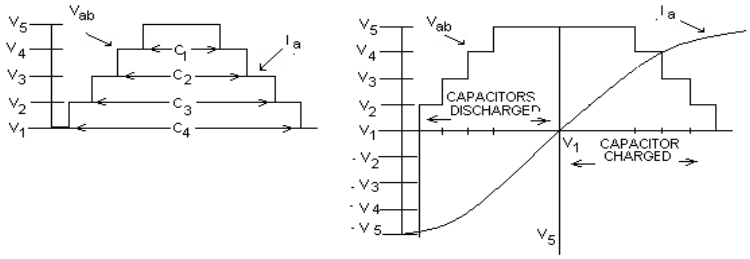

Figure 3: Waveforms Showing Capacitor Charging Profile (a) Voltage and Current in Phase (b) Voltage and Current Are 90^0 Out of Phase.

Multilevel Converter Topologies

The general objective of the multi-level converter is to synthesize a sinusoidal voltage form several levels of voltages by constructing a staircase kind of wave shape. Typically the different voltage levels are obtained from several capacitors connected in series across a DC bus the minimum number of levels of voltage in a multi-level inverter is three.

Basic multi-level topologies have been categorized into the following three types (1) Diode clamped; (2) Flying capacitor; and (3) Cascaded inverter topologies.

PWM Classification

There are many possible PWM techniques proposed in the literature. The classifications of PWM techniques can be given as follows:

1. Sinusoidal PWM
2. Space-Vector PWM
3. Hysteresis band current control PWM

V. Space Vector Pulse Width Modulation (SVPWM)

The space vector pulse width modulation method is an advanced, computation intensive PWM method, which is an excellent feature and is possibly the best among all the PWM techniques for variable frequency drive applications. It has been found wide spread application in recent years, because of its superior performance characteristics.

The space vector pulse width modulation (SVPWM) technique is more popular than conventional technique because of the following excellent features: It achieves the wide linear modulation range associated with PWM, third-harmonic injection automatically.

- It has lower base band harmonics than regular PWM or other sine based modulation methods, or otherwise optimizes harmonics.
- 15% more output voltage than sinusoidal modulation, i.e. better dc-link utilization.
- More efficient use of dc supply voltage.
- Advanced and computation intensive PWM technique.
- Higher efficiency.
- Prevent un-necessary switching, hence less commutation losses.
- A different approach to PWM based on space vector representation of the voltages in the reference frame transformation.

The space vector concept is derived from the rotating field of AC machine which is used for modulating the inverter output voltage. In this modulation technique, the three phase quantities can be transformed to their equivalent two-phase quantity either in synchronously rotating frame (or) stationary frame. From this two-phase component the magnitude of reference vector can be found and is used for modulating the inverter output. The process of obtaining the rotating space vector is explained in the following section, considering the stationary reference frame.

Let the three-phase sinusoidal voltage component be,

$$V_a = V_m \sin wt \quad (2)$$

$$V_b = V_m \sin(wt - 2\pi/3) \quad (3)$$

$$V_C = V_m \sin(wt + 2\pi/3) \quad (4)$$

When this three-phase voltage is applied to the AC machine, it produces a rotating flux in the air gap of the AC machine. This rotating flux component can be represented a single rotating voltage vector. The magnitude and angle of the rotating vector can be found by means of Clark's Transformation as explained below in the stationary reference frame. The representation of rotating vector in Complex plane is shown in Fig.

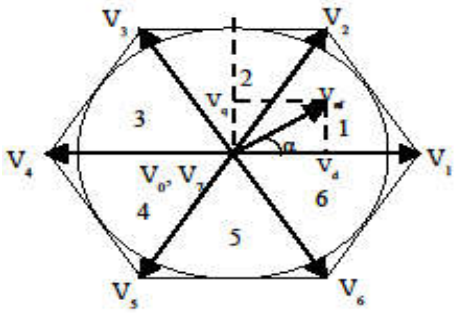

Figure 4: Representation of Rotating Vector in a Complex Plane Space Vector Representation of the Three-Phase Quantity

$$\left|\overline{Vref}\right| = V_d + jV_Q + 2/3(V_a + aV_b + a^2c) \quad (5)$$

Where a=$e^{j2\pi/3}$

$$\left|\overline{Vref}\right| = \sqrt{V_d^2 + V_q^2} \; ; \alpha = \tan^{-1}\frac{V_d}{V_q} \quad (6)$$

$$V_d + jV_q = 2/3\left(V_a + e^{\frac{j2\pi}{3}} V_b + e^{-\frac{j2\pi}{3}} V_C\right) \quad (7)$$

$$V_d + jV_q = \frac{2}{3}\left(V_a + \cos\frac{2\pi}{3}V_b + \cos\frac{2\pi}{3}V_c\right) + j\frac{2}{3}\left(\sin\frac{2\pi}{3}V_b + \sin\frac{2\pi}{3}V_c\right) \quad (8)$$

The equation in the matrix form can be written as:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (9)$$

The Space vector PWM treats the sinusoidal voltage as a constant amplitude vector rotating at a constant frequency. This PWM technique approximates the reference voltage V_{ref} by a combination of the eight switching patterns. A three-phase voltage vector is transformed into a vector in the stationary d-q co-ordinate frame. This represents the spatial vector sum of the three-phase voltage.

VI. Proposed Methodology

The proposed topology includes a dc-link that is common among the three phases. The dc-link provides three voltage levels +2E, 0, and -2E for the phase legs. Since all the phases have similar configuration, only one phase leg of the proposed topology has been shown in Fig. 5. All the components shown in the figure have equal operating voltage E i.e. one fourth of the dc-link voltage V_{dc}. The flying capacitors C_{A1} and C_{A2} are controlled to stay charged at the target voltage E.

The available states of one phase leg are shown in table 1. To generate level 2E, all the top arm switches S_{A1}, S_{A2}, S_{A3}, S_{A4} should turn on. For level E, two choices are available i.e. either through dc-link's positive point (EP) or through dc-link's neutral point (E0). This redundancy can be used to balance the voltage of C_{A1}. Level 0 is generated through clamping the dc- link's neutral point to the output (00). Negative states can be generated similarly due to the symmetry of the topology.

The operation of this topology is in essence similar to topologies such as stacked multi cell (SMC) converter, where the positive and negative stacks operate independently. Hence, the positive stack capacitor C_{A1} is used and balanced during the positive cycle and rest during the negative cycle, whereas the negative stack capacitor C_{A2} is used and balanced during the negative cycle and rest during the positive cycle. So, the flying capacitors will see the switching frequency rather than line frequency and therefore the capacitor size is not too large.

Similar to the three-level NPC inverter, if the three phases of the load are balanced, the neutral point voltage will be constant in theory. However, the voltage might slightly drift away due to the imbalance in the elements' leakage current. In addition, although small, there is always some imbalance among the phases. A constant voltage drift, even though small, can cause higher voltage across part of the devices which can be lethal. Nevertheless, this drift can be compensated by injecting a small common mode to the three phases.

An important feature of the proposed topology is the even distribution of transitions among switching devices. Therefore, switching loss which is the major limiting factor of inverter's thermal performance is distributed among the switches. As the main result, the tradeoff between switching frequency and current derating is improved. This provides the opportunity to either increase the rated current and power of the inverter or increase the switching frequency resulting in lower capacitor size and improved voltage waveform quality.

Modulation Techniques

Various modulation techniques may be adapted for the proposed topology. Carrier-based modulation with sinusoidal or modified reference as well as non-carrier-based techniques such as space vector modulation and selective harmonic elimination may be used to generate the gate signals. The choice of a modulation technique is mostly a tradeoff among the requirements of the application

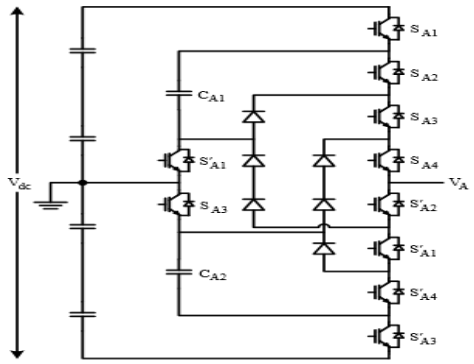

Figure 5: A Phase Leg of the Proposed 5-Level Hybrid Topology

Table 1: Switching States of the Proposed Inverter

Level	State	S2	S3	S4	C1	C2
+2E	+2E	1	1	1	N.A.	N.A.
+E	+EP	0	1	1	i>0 Charge i<0 Discharge	N.A.
	+E0	1	1	1	i>0 Discharge i<0 Charge	N.A.
0	0	0	1	1	N.A.	N.A.
-E	-E0	0	1	0	N.A.	i>0 Charge i<0 Discharge
	-EN	0	0	1	N.A.	i>0 Discharge i<0 Charge
-2E	-2E	0	0	0	N.A.	N.A.

CARRIER-BASED MODULATION

Carrier set's arrangement and reference waveform's shape are the main sources of varieties in carrier-based modulation techniques for multilevel inverters.

As for carrier set's arrangement, level shifted carriers LSC and phase shifted carriers PSC are the two main categories that are respectively suitable for diode-clamped and multi-cell structures. Two members in the LSC family, alternative phase opposition disposition APOD and phase disposition PD are known to generate the best results for singe-phase and three- phase applications, respectively. PSC in its original form has been shown to generate a PWM waveform that matches with APOD. Also a modified version of PSC with dynamic phase shift has been shown to match with PD [16].

The reference for single-phase applications is usually a simple sinusoidal waveform. For three-phase applications, a variety of reference waveforms are available due to the possibility of common mode injection in three-phase structure. This flexibility has been used to serve different purposes such as increased dc link utilization, lower THD, lower Loss, and neutral point voltage control.

For the proposed inverter, a hybrid modulation technique is required due to the hybrid structure of the topology. Figure below illustrates the modulation technique for single-phase case. It is intuitive to separate the operation to positive and negative cycles, since each cycle is generated with a 3-level FC stack. The gate signals for each FC is then generated using PSC to provide natural voltage balancing for the flying capacitors. The generated output

PWM waveform matches the APOD scheme

For three-phase case, similar approach may be adopted except that, to generate a PD scheme equivalent, the positive cycle carriers should have π/2 phase shift compared to the negative cycle carriers. Also, the carriers incorporate a dynamic phase shift which for sampled reference waveforms always adds up by π/2 at the carrier band transitions. For the reference waveform, centered space vector PWM (CSVPWM) sampled at half PD carrier period can provide similar output performance as SVM. Figure 4 illustrates the modulation technique using sampled CSVPWM along with modified PSC for the proposed inverter.

NON-CARRIER-BASED MODULATION

For non-carrier-based modulation techniques such as SVM and SHE, the output PWM waveform may be generated first and then decomposed to the required switching signals. Figure below illustrates the required procedure to generate the gate signals for each phase leg. The 5-level PWM waveform is first separated to positive and negative cycle 3-level PWMs. Using state machine decoder, each cycle is then decomposed to two 2-level PWMs i.e. the required gate signals for each FC cell.

It is important to note that this procedure is independent of the adopted modulation technique. Therefore, it can be used with carrier-based modulation techniques as well as non- carrier-based. This might be a good alternative when the complexity of the carrier-based technique is relatively high e.g. for PD scheme.

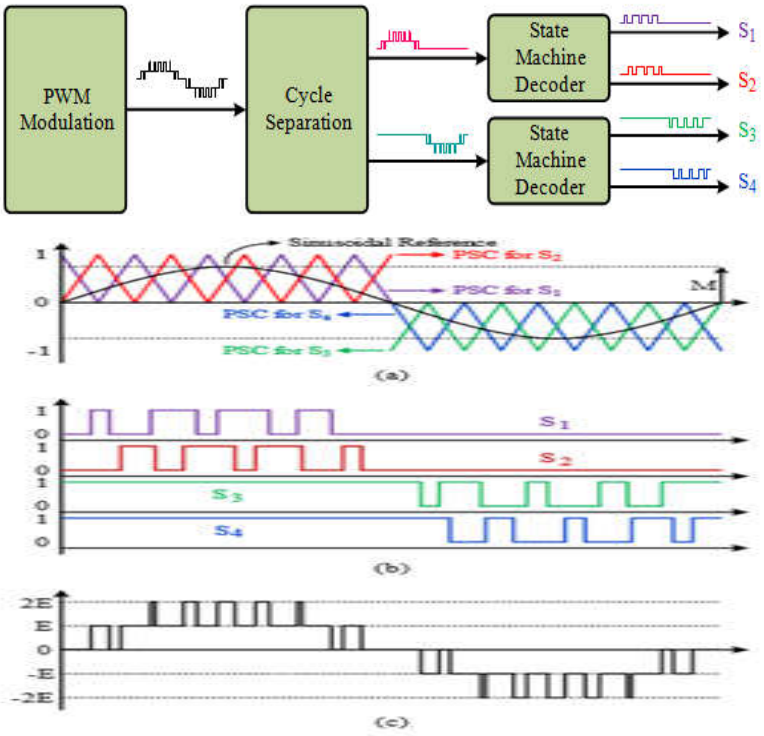

Figure 6: Carrier-Based Modulation using PSC with Sinusoidal Reference for Single Phase Application (a) Reference and Carriers Arrangement (b) Gate Signals (c) Output Waveform

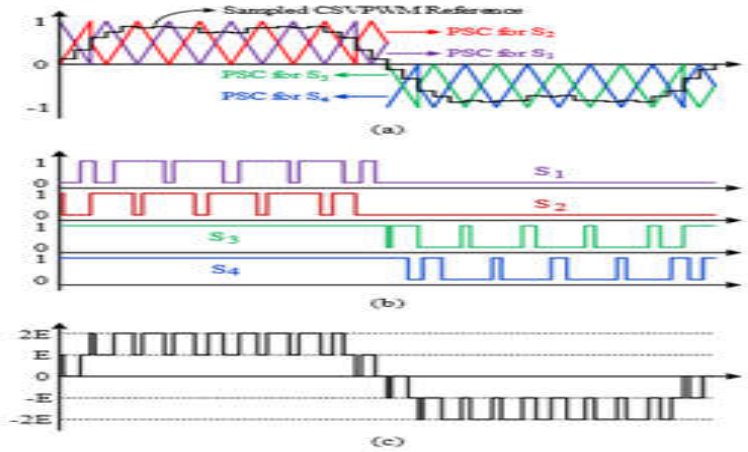

Figure 7: Carrier-Based Modulation using Modified PSC with Sampled CSVPWM Reference for Three Phase Application (a) Reference and Carriers Arrangement (b) Gate Signals (c) Output Waveform

VII. *Simulation Result*

For validation of proposed work here MATLAB/Simulink based model is shown in figures below shows the parameter used in the Simulink.

This designing is conducted in given stages:

1. MATLAB Simulation of five level neutral point flying capacitor using space vector modulation technique.
2. MATLAB Simulation of five level neutral point flying capacitor using sinusoidal pulse width modulation technique.

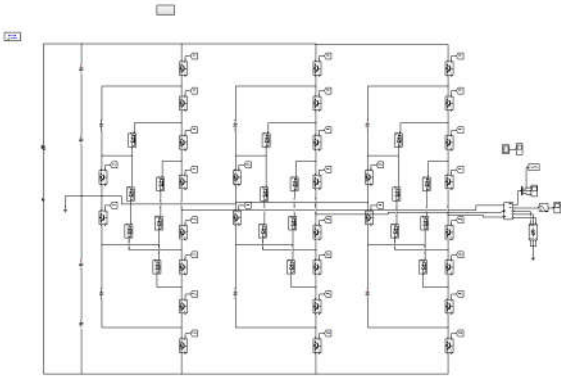

Figure 8: The Proposed Hybrid Active Neutral Point Five Level Flying Capacitor using SPWM Topology

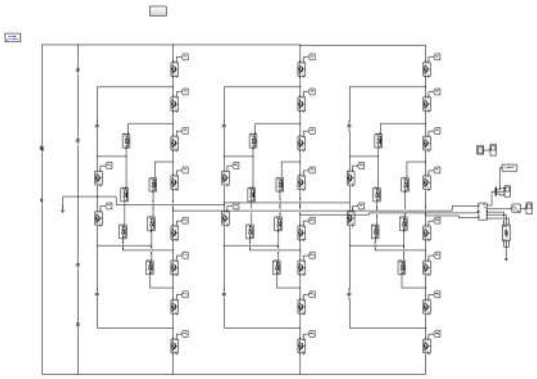

Figure 9: The Proposed Hybrid Active Neutral Point Five Level Flying Capacitor using SVPWM Topology

The above is the modeling of hybrid active neutral point converter clamped flying capacitor multilevel inverter with three phases. Each phase comprises of 10 IGBTs operating in synchronization with 120 degrees phase delay to each other. The flying capacitors used have capacity of 330uF each. The upper and lower switches are complimentary which operate using NOT gate for switching operation.

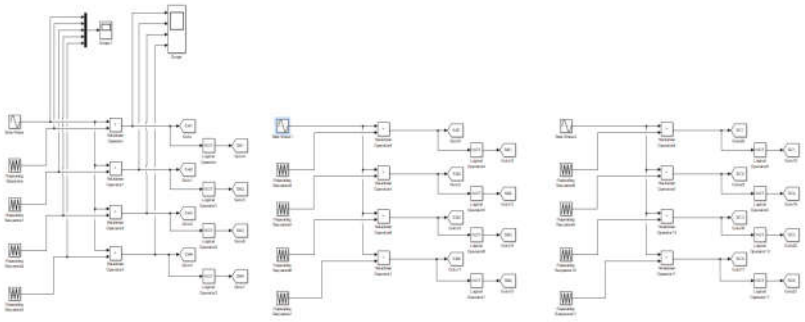

Figure 10: Signal Generator Control for IGBTS using Simple Sinusoidal PWM Technique

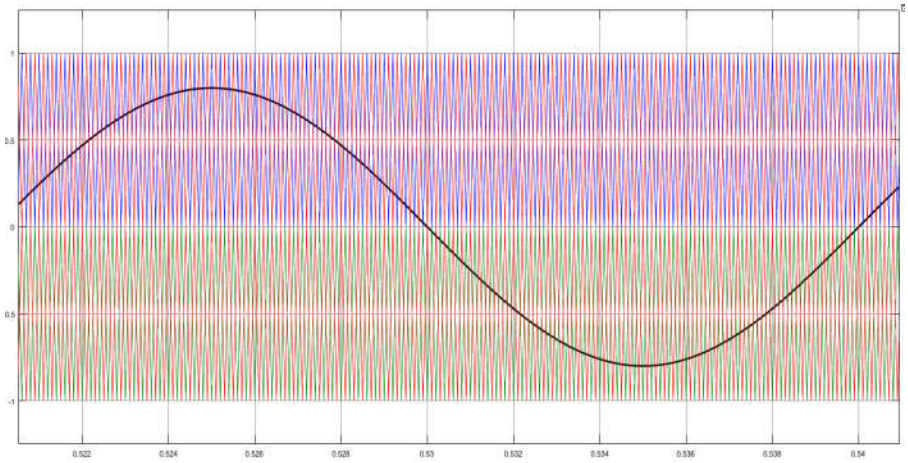

Figure 11: Sinusoidal Comparison to High Frequency Triangular Waveform

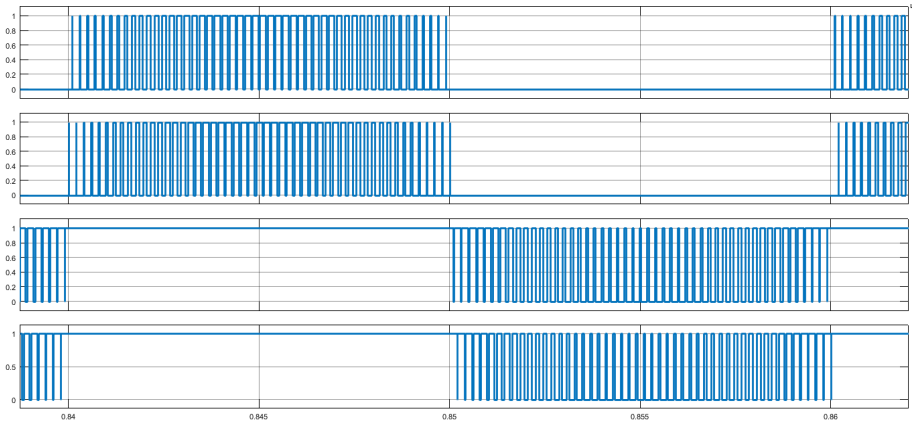

Figure 12: Pulses for the Upper Region Switches

The pulses generated for the upper region switches with comparison of four level shifted high frequency triangular waveforms are connected to NOT gate to generate pulse for lower region switches. The output generated after the pulses are fed to the IGBT switches is shown below.

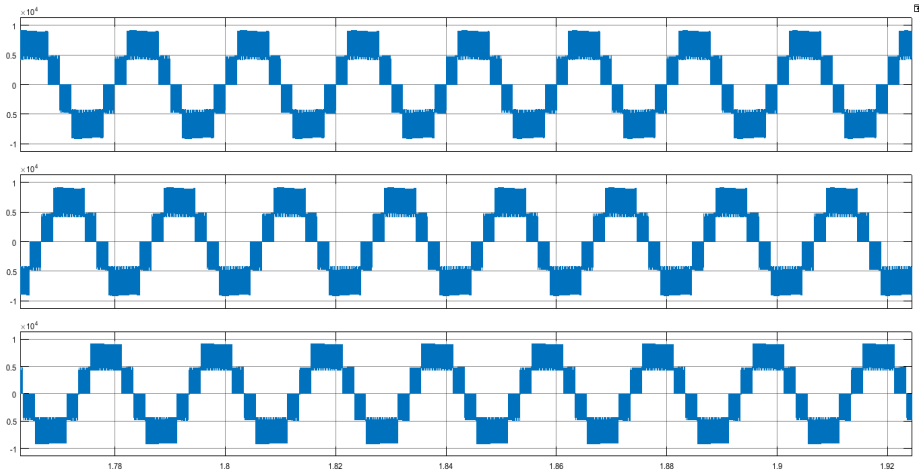

Figure 13: Five Level Output Voltages of Phase abc using Sinusoidal PWM Technique

The flying capacitor voltages are shown below;

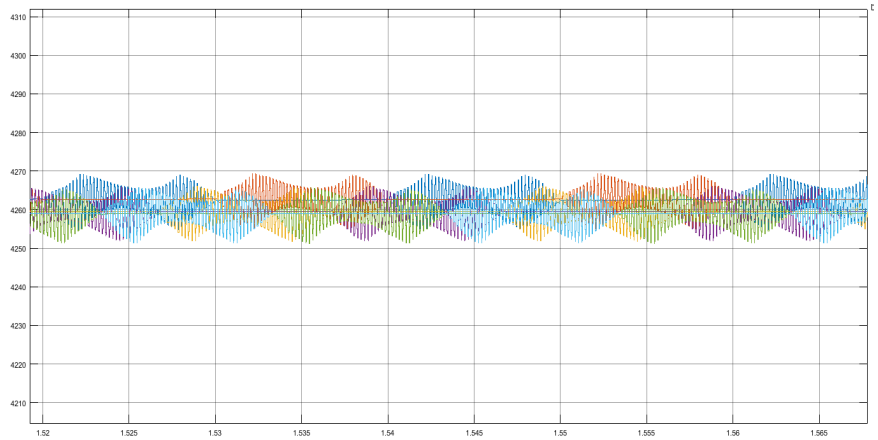

Figure 14: Flying Capacitor Voltages with SPWM Technique

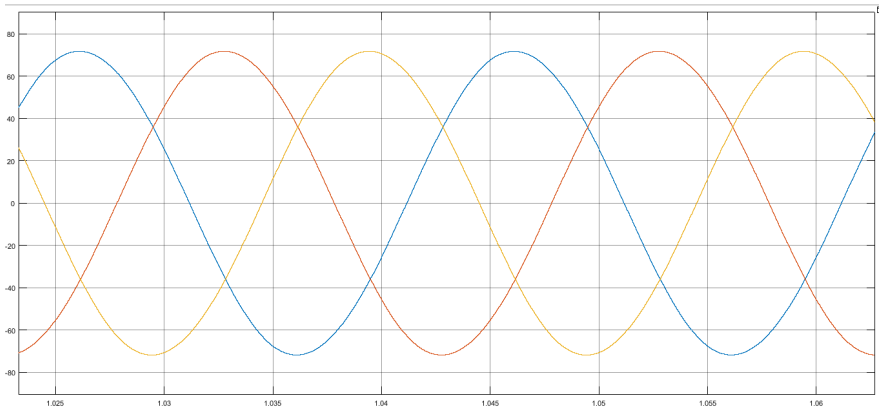

Figure 15: Load Current with Resistive Load in SPWM

The current is pure sinusoidal for the given input from the multilevel inverter. The modeling is updated with carrier based space vector PWM technique with no change in the IGBT connections or the topology. The carrier based space vector PWM is shown below.

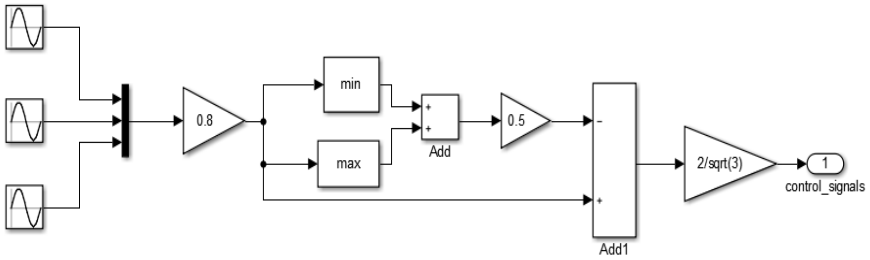

Figure 16: Carrier Based Space Vector PWM Technique Modeling

In the above modeling the sinusoidal waveforms are taken as input for generation space vector signals. The space vector generation is done from

Vsv = Voffset - (Vmax + Vmin)/2

The control signals are compared to four level shifted high frequency triangular waveforms generating pulses for upper region switches similar to the previous topology. The output voltages are recorded and compared with the previous topology.

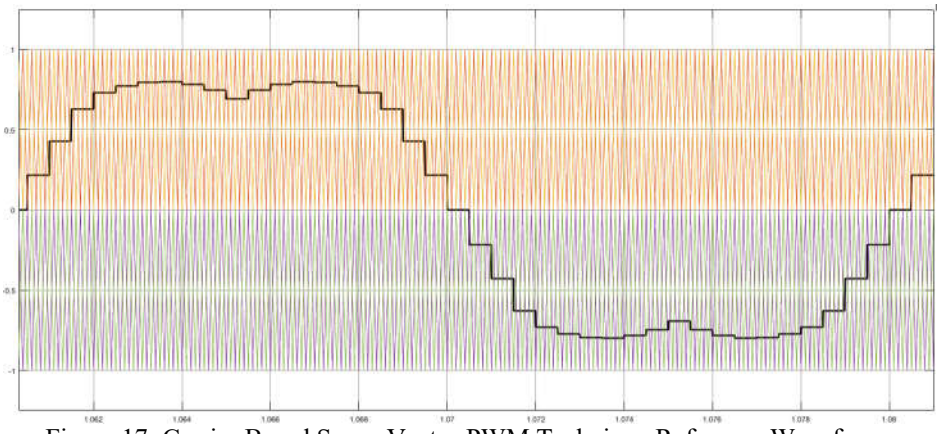

Figure 17: Carrier Based Space Vector PWM Technique Reference Waveforms

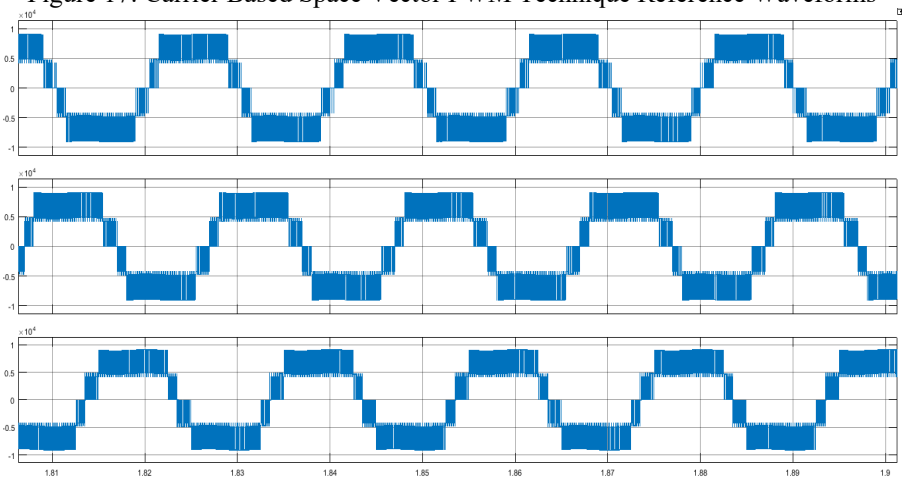

Figure 18: Five Level Output Voltages of Phase abc using CSV PWM Technique

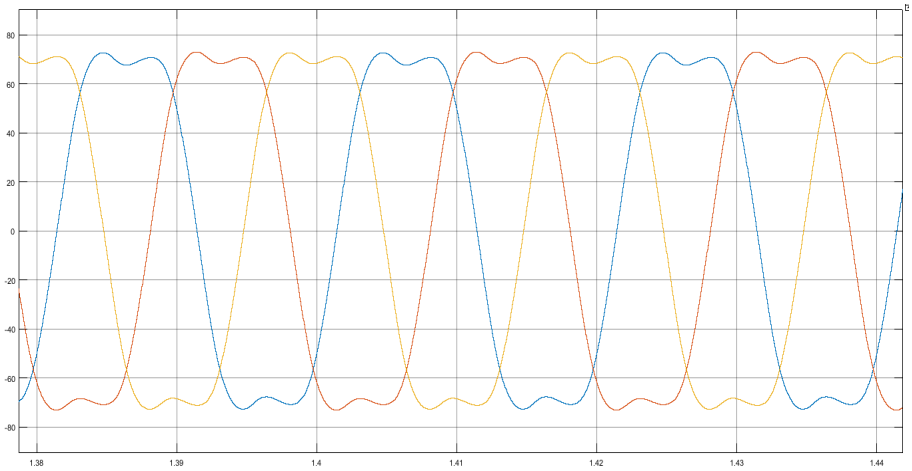

Figure 19: Load Current with Resistive Load in CSV PWM

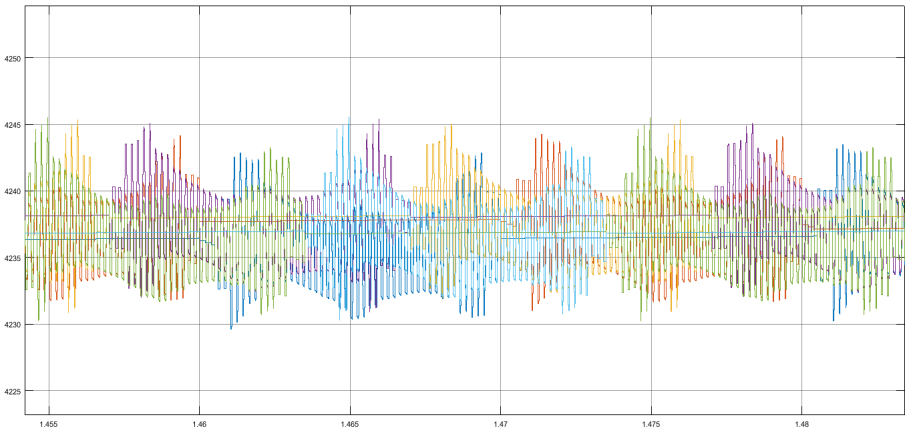

Figure 20: Flying Capacitor Voltages with CSV PWM Technique

The results are compared using FFT analysis tool for the voltage magnitude and THD of both the voltages with SPWM and CSV PWM.

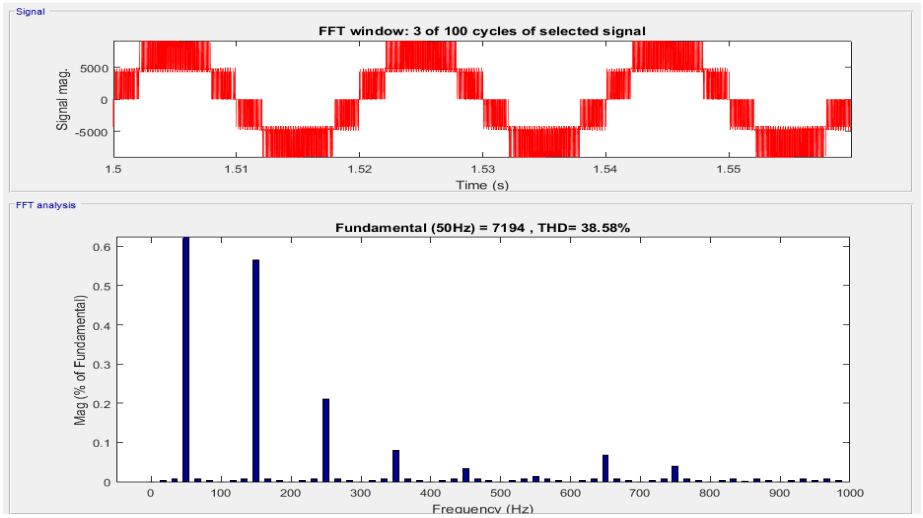

Figure 21: THD of the Voltage Waveform with SPWM Technique

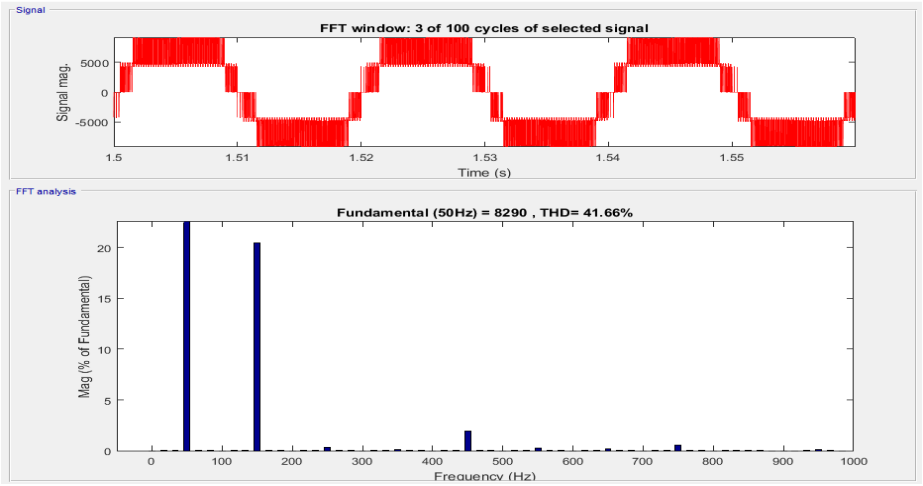

Figure 22: THD of the Voltage Waveform with CSV PWM Technique

Conclusion

Recent trend in power electronics is based on the use of multilevel inverter technology. Multilevel inverter uses so many switches for generating output. Each switch produces loss in the power. This gives low power at the output. So need for some special topology which have low switch. As observed the voltage amplitude of the voltage with SPWM technique is recorded at 7194V and for the CSV PWM technique it is recorded at 8290 with an increase of approximately 1100V. However, the THD of the CSV PWM is analyzed at 41.66% and SPWM is analyzed at 38.58%. This has not much change. The increase of 1100V is considered to be higher change as compared to increase in THD with only 3% increase. The CSV PWM technique is more advantageous as compared to SPWM with increased voltage amplitude of 1100V and very less increment of THD.

References

[1] H. Abu-Rub, J. Holtz, and J. Rodriguez, “Medium-Voltage Multilevel Converters—State of the Art, Challenges, and Requirements in Industrial Applications,” IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2581–2596, Aug. 2010.

[2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, J. Rodriguez, M. A. Pérez, and J. I. Leon, “Recent Advances and Industrial Applications of Multilevel Converters,” IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[3] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A Survey on Cascaded Multilevel Inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[4] J. Rodriguez, "Multilevel inverters: a survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.

[5] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[6] B. P. McGrath, T. Meynard, G. Gateau, and D. G. Holmes, "Optimal Modulation of Flying Capacitor and Stacked Multicell Converters Using a State Machine Decoder," IEEE Trans. Power Electron., vol. 22, no. 2, pp. 508–516, Mar. 2007.

[7] H. Sepahvand, M. Khazraei, K. Corzine, and M. Ferdowsi, "Startup Procedure and Switching Loss Reduction for a Single-Phase Flying Capacitor Active Rectifier," Ind. Electron. IEEE Trans., vol. 60, no. 9, pp. 3699–3710, May 2013.

[8] T. Bruckner, S. Bernet, and H. Guldner, "The Active NPC Converter and Its Loss-Balancing Control," IEEE Trans. Ind. Electron., vol. 52, no. 3, pp. 855–868, Jun. 2005.

[9] S. R. Pulikanti and V. G. Agelidis, "Hybrid Flying-Capacitor-Based Active-Neutral-Point-Clamped Five-Level Converter Operated With SHE-PWM," IEEE Trans. Ind. Electron., vol. 58, no. 10, pp. 4643– 4653, Oct. 2011.

[10] M. Narimani, B. Wu, Z. Cheng, and N. Zargari, "A New Nested Neutral Point Clamped (NNPC) Converter for Medium-Voltage (MV) Power Conversion," IEEE Trans. Power Electron, vol. 8993, no. pp. 1–1, 2014.

[11] T. B. Soeiro and J. W. Kolar, "The New High-Efficiency Hybrid Neutral-Point-Clamped Converter," IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 1919–1935, May 2013.

[12] F. Kieferndorf, M. Basler, L. a. Serpa, J.-H. Fabian, a. Coccia, and G. a. Scheuer, "A new medium voltage drive system based on ANPC-5L technology," 2010 IEEE Int. Conf. Ind. Technol., pp. 643–649, 2010.

[13] G. Gateau, T. A. Meynard, and H. Foch, "Stacked multicell converter (SMC): properties and design," in 2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230), 2001, vol. 3, pp. 1583–1588.

[14] T. A. Meynard, H. Foch, F. Forest, C. Turpin, F. Richardeau, L. Delmas, G. Gateau, and E. Lefeuvre, "Multicell converters: derived topologies," IEEE Trans. Ind. Electron., vol. 49, no. 5, pp. 978–987, Oct. 2002.

[15] R. Naderi and A. Rahmati, "Phase-Shifted Carrier PWM Technique for General Cascaded Inverters," IEEE Trans. Power Electron, vol. 23, no. 3, pp. 1257–1269.

[16] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[17] Sridhar R. Pulikanti, Georgios Konstantinou, Graduate Student, and Vassilios G. Agelidis, Senior, Transactions on industrial electronics, vol. 60, no. 11, november 2013.

[18] Javier chivite-zabalza, pedro izurza-moreno, danel madariaga, gorka calvo, and miguel angel rodr´ıguez, , ieee transactions on power electronics, vol. 28, no. 10, october 2013.

[19] Anshuman shukla , arindam ghosh, and avinash joshi, ieee transactions on industrial electronics, vol. 57, no. 7, july 2010.

[20] K. siva kumar, Anandarup das Rijil ramchand, Chintan patel, and k. gopakumar, ieee transactions on industrial electronics, vol. 57, no. 11, november 2010.

[21] A

. Hamerli and B. Odegard, “AC excitation with ANPC: ANPC converter technology tailored to the needs of AC excitation equipment for pump storage plants,” ABB Rev., vol. 3, pp. 40–43, 2008.

[22] D. Floricau, E. Floricau, and G. Gateau, “Three level active NPC converter: PWM strategies and loss distribution,” in Proc. IEEE IECON, 2008, pp. 3333– 3338.

[23] N. Flourentzou, V. G. Agelidis, and G. Demetriades, “VSC based HVDC power transmission systems: An overview,” IEEE Trans. Power Electron., vol. 24, no. 3, pp. 592–602, Mar. 2009.

[24] L. Ma, T. Kerekes, R. Teodorescu, X. Jin, D. Floricau, and M. Liserre, “The high efficiency transformer-less PV inverter topologies derived from NPC topology,” in Proc. EPE, 2009, pp. 1–10.

[25] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. Portillo, M. Prats, and M. Perez, “Multilevel converters: An enabling technology for high-power applications,” Proc. IEEE, vol. 97, no. 11, pp. 1786– 1817,Nov. 2009.