FPGA Implementation of Chirp Acoustic Modem using DDS for Underwater Wireless Communication

J.Kamalakar[1], D.B.V.Jagannadham[2]

[kamal.jayanthy@gmail.com]

PG Student (M. Tech-VLSI & Embedded Systems**)**, Department of E.C.E, Gayatri Vidya Parishad College of Engineering (A), Visakhapatnam, India[1]

Professor, Department of E.C.E, Gayatri Vidya Parishad College of Engineering (A), Visakhapatnam, India[2]

Abstract*—Underwater Wireless Communication is a trending field of research and engineering in recent years. The transmission of information in underwater media can be based on acoustic systems, which present the advantage that the acoustic waves have lower absorption than the electromagnetic ones. The terrestrial Communication and Signal processing techniques for improving the range and data rate for UWA channels cannot meet the existing underwater environmental constraints. One of the recommended methods is by generating the Dolphin sounds such as Linear Frequency Modulated Signals (LFM) also called as Chirp signals. This thesis emphasis on generation of LFM (Chirp) signals using Digital Directed Synthesis (DDS-AD9834) chip which is interfaced with FPGA. The paper illustrates the function of AD9834 DDS signal generator by Direct Digital Synthesized (DDS) modulated LFM (Chirp) signals and testing the performance. Further this paper intends to implement indigenously developed programmable Underwater Chirp Acoustic Modem which is a device that typically consists of transducer interface card with ZYNQ 7000 Programmable System on Chip Field Programmable Gated Array (FPGA) to perform digital communication operations. The DDS integrated with Chirp acoustic modem is used for wireless design, simulation and analysis using Xilinx VIVADO design suite. This paper reflects the implementation of complete DDS-AD9834 integrated with Chirp acoustic modem using Model Based FPGA design standards with custom generated Chirp signals.*

Keywords: Underwater Acoustic Wireless communication, Linear Frequency Modulated (LFM), Chirp Slope Keying (CSK), Direct Digital Synthesis (DDS), Field Programmable Gated Array (FPGA).

I. INTRODUCTION

There is an enormous demand for underwater wireless communication with the booming expansion in marine environmental monitoring activities. The necessity for underwater wireless communications exists in a broad range of applications, such as sensor-based, including ocean sampling networks, under sea explorations, disaster prevention, and navigation assistance, speech transmission between divers, distributed tactical surveillance, and mine reconnaissance, remote control in off-shore oil industry, pollution monitoring in environmental systems, collection of scientific data recorded at ocean-bottom stations and mapping of the ocean floor for detection of objects, as well as for the discovery of new resources. Wireless underwater communications can be established by transmission of acoustic waves. Underwater communication requires high-speed data rates over a relatively long distance, in terms of kilometers, in a shallow water environment.

Underwater communications, which is exclusively for military at one time, is being extending now into commercial fields. The possibility to maintain signal transmission enables gathering of data from submerged instruments without human intervention, and unobstructed operation of unmanned or autonomous underwater vehicles (UUV's, AUV's) are different types of communications. The disadvantage with underwater wired communication is that the cables are easily damaged, by travelers and other under water activity. In addition, the vehicle connected to the cables must

have additional power to drag the cable through the water. Underwater wireless acoustic communications helps us to eliminate physical connection of wires.

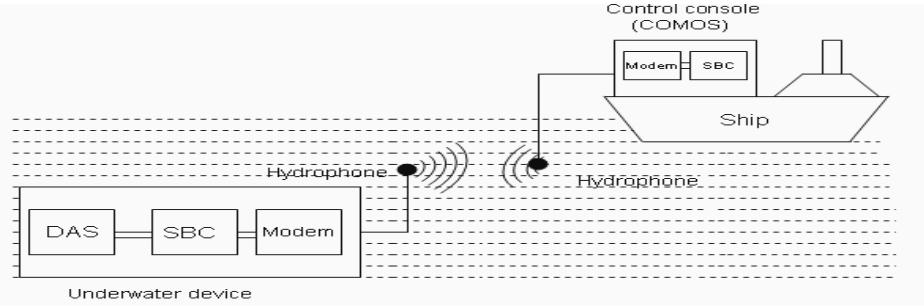


Fig.1: Base station Modem (Ship) and Chirp Acoustic Modem setup

In this paper, the overall wireless communication setup has been established using two identical custom made high performance ZYNQ FPGA hardware oriented chirp acoustic modems namely (Underwater Chirp Acoustic Modem and Base Station Chirp Acoustic Modem) where both of them are interfaced with AD9834 DDS chip which will be used as a powerful signal generator component.

The Chirp signals (Linear Frequency Modulated) signals are used as main entity for signal transmission and reception purpose and preferred due to its high range resolution, effective target range detection scope, lower latency; lesser multipath spread and improvised autocorrelation properties.

II. DIRECT DIGITAL SYNTHESIZER(DDS-AD9834)

Direct digital synthesizer is a device which produces an analog waveform (Sine waveform) by generating a time varying signal in digital (binary) format and then converting the digital signal into an analog signal using a Digital to Analog convertor (DAC) [1]. In this paper, a programmable AD9834 DDS which is of 75MHz, 20 mW low consumption power at 3V device is used to generate desired chirp (LFM) signals.

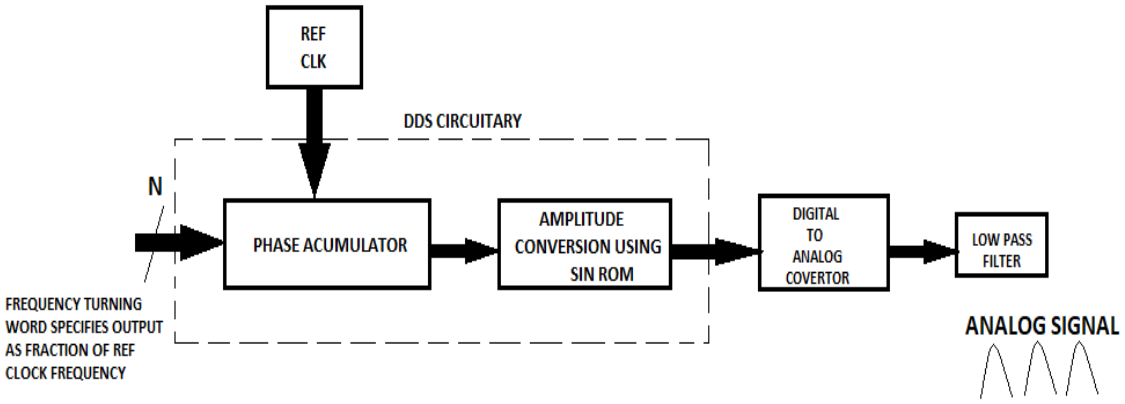


Fig.2: Bock diagram of Direct Digital Synthesis.

DDS Operation: The above figure Fig.2 illustrates the basic building blocks of DDS technology where it converts the digital signals into analog signals using a DAC. Direct Digital Synthesizer (DDS) generally consists of phase accumulator, ROM for storing sine values, 10 Bit-D/A converter along with a low pass filter (LPF). A DDS generates a sine wave at a given frequency. The frequency depends on two variables, the reference-clock frequency and the binary number programmed into the frequency register (tuning word). The binary number in the frequency register provides the main input to the phase accumulator. The DDS AD9834 works on the below equation,

$$F=\Delta Phase \times F_{MCLK}/2^{28}$$
$$\text{Where } 0 < \Delta Phase < 2^{28}-1$$

where input to the phase accumulator is selected by configuring the frequency registers and the accumulator simply scales the range of phase numbers into a multibit digital word. The contents of the phase accumulator (digital phase

values) are stored as a lookup table in the SIN ROM and it converts phase information into amplitude. The DAC, in turn, converts that number to a corresponding value of analog voltage or current and output analog signal is appeared at the low pass filter [1],[3].

III. CHIRP SLOPE KEYING(CSK) MODULATION SCHEME

Chirp modulation or Linear Frequency Modulation is a scheme where the signal is spread through entire bandwidth from one end to other in the sinusoidal waveform which varies with respect to time. The signal frequency is swept form up to down and vice versa and in turn termed as Up chirp and Down chirp signals denoting with binary '1' for up chirp and '0' for down transitions respectively. The digital data is transmitted over the slope of the chirp signals in the above mentioned procedure in order to achieve effective transmission and reception in the underwater wireless acoustic communication environment [4,13].

The standard time-domain expression for a sinusoidal linear chirp signal may be expressed as

$$S(t) = \cos[2\pi fo\ t + \pi \boldsymbol{\mu} t^2 + \Theta_o] \text{------ (1)}$$

Where' $\mathbf{f_0}$ is the starting frequency at (time =0), and the Chirp rate of frequency increase or decrease defined as

$$\boldsymbol{\mu} = \frac{Fmax - Fmin}{tmax - tmin}$$

where the Bandwidth and Time interval is given by,

$$B = f_{max} - f_{min} \text{ and } \Delta t = t_{max} - t_{min}$$

In this paper, the chirp signals for range of 12 KHz to 17 KHz are generated using DDS device and are programmed using VHDL coding, functionally verified with Xilinx VIVADO software tool.

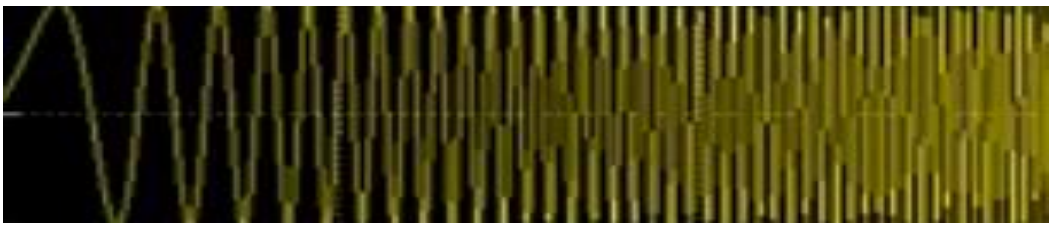
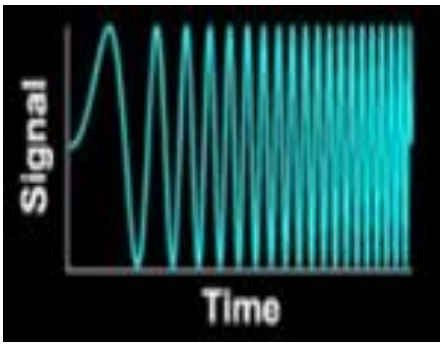
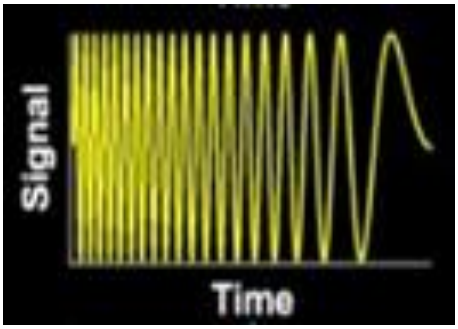


Fig.3 The DDS generated Chirp (LFM) signal



3a) Up Chirp Signal



3b) Down Chirp signal

The above figures (Fig 3a, Fig3b) are the basic representation of the up & down chirp signals
The below mentioned equations (2) and (3) are the standard representation of Up chirp & Down chirp equations respectively:

$$S_{cu}(t) = \exp[\ 2\pi t(\ f_{max} - f_{min}\ )/T \times t\ + f_{min}] \quad \text{----(2)}$$

$$S_{cd}(t) = \exp[\ 2\pi t(\ f_{min} - f_{max}\ )/T \times t\ + f_{max}] \quad \text{----(3)}$$

IV.ACOUSTIC MODEM DESIGN USING FPGA HARDWARE

Hardware implementation plays a crucial role where the two different modems which are placed at certain distance have to be configured and controlled from base station using wireless signal commands. Initially, the underwater hardware design is a customised FPGA setup which consists of a Data Acquisition system, Single board computer, acoustic sensor and Chirp acoustic Modem. The underwater acoustic analog signals are captured by the sensor, accumulated and further processed by Data acquisition system. The processed signal is then modulated by DDS signal generator and transmitted through a hydrophone.

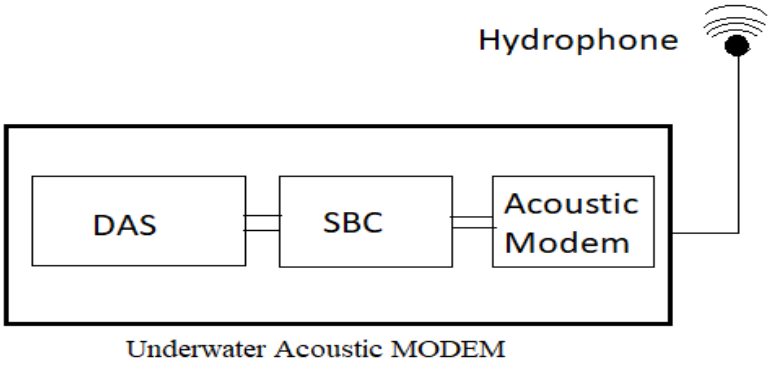


Fig.4: Block diagram of Underwater Chirp Acoustic Modem.

The Base station Modem setup is also a Chirp acoustic modem which is equipped with ZYNQ 7000 all programmable System on chip FPGA hardware where the data or signals acquired from underwater Chirp acoustic modem are further processed; monitored and necessary action is taken according to the received data by passing the commands accordingly. The data from underwater modem to base station modem and vice versa is continuously monitored and thus the actual wireless communication strategy is established at underwater environment.

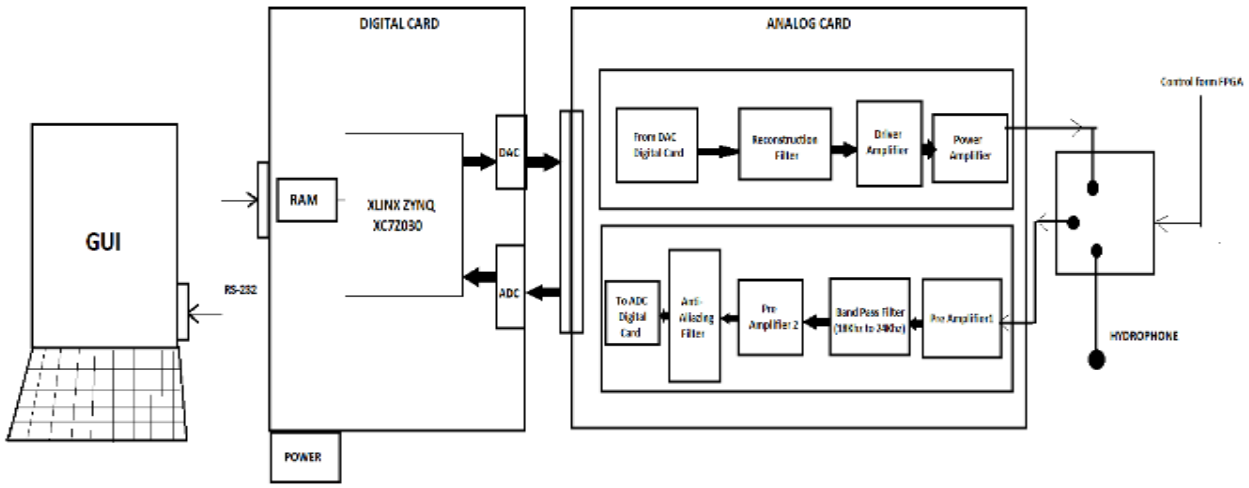


Fig.5: Internal blocks of Base station Chirp Acoustic Modem

The ZYNQ is of Harvard architecture, from the latest generation of Xilinx's family which combines both the software programmability features of ARM based processor and FPGA(hardware) on a single chip, where the overall cost and physical size of the device reduces. The Zynq FPGA consists of two dual core ARM Cortex A-9 processors, Processing System unit, Programmable Logic unit and other advanced extensible interface (AXI) which enables high performance and low latency to the entire system. The Processing system unit equipped with application processor unit, memory interfaces, I/O peripherals and interconnects and the Programmable logic units deals with all the configurable logic blocks, slices, RAM, ADC, programmable I/O blocks and LUTs

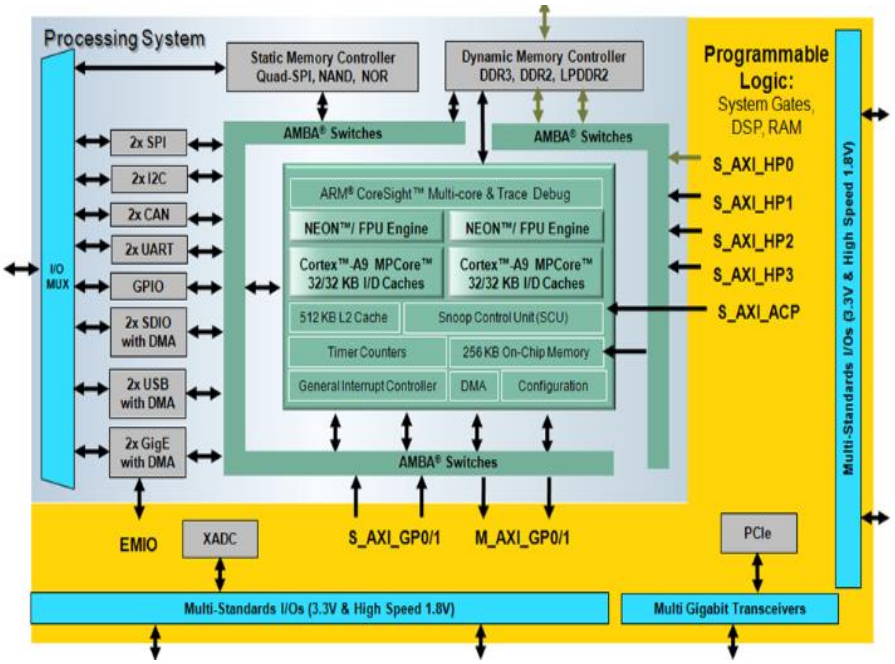


Fig.6: Zynq 7000 FPGA architecture diagram

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V.RESULTS AND DISCUSION

The Chirp (LFM) signals are modulated by conjuring the DDS source code module in such a way that the desired frequency range from 12KHz to 17KHz is coded in state machine format where 'CLK_STATE', 'CSK_CLK' and 'CSK_CONFIG' are considered to be main processing parameters. The DDS reference clock is fixed for 50MHz and upon configuring all the frequency words in the code for all the 12 states, the below simulation results are generated (Fig.7, Fig.8 & Fig.9).After confirmation of simulation results, the entire design is then processed for synthesis and reports are generated. The post synthesis procedure, the entire design is processed for Bit file generation, it is dumped on to the target FPGA (Chirp Acoustic Modem) and the final output of the system is observed on an oscilloscope.Post analysis of the target results, the entire design module is processed for IP generation and an IP module is generated with VIVADO IP Creator feature.

1. Simulations: The Chirp slope keying modulation is coded using VHDL and the DDS is configured with all the frequency words ranging from 12KHz to 17 KHz accordingly and it is simulated using Xilinx VIVADO Design suite tool.

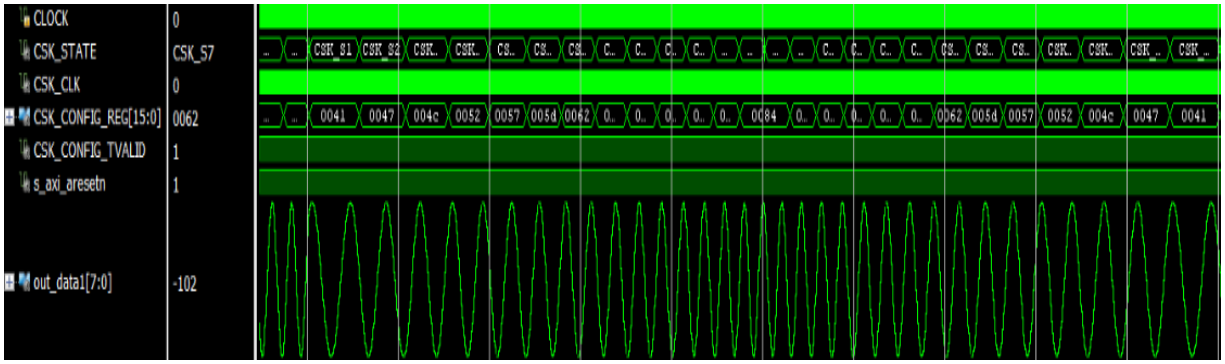

Fig.7: Chirp signals simulation sweeping from 12KHz to 17 KHz.

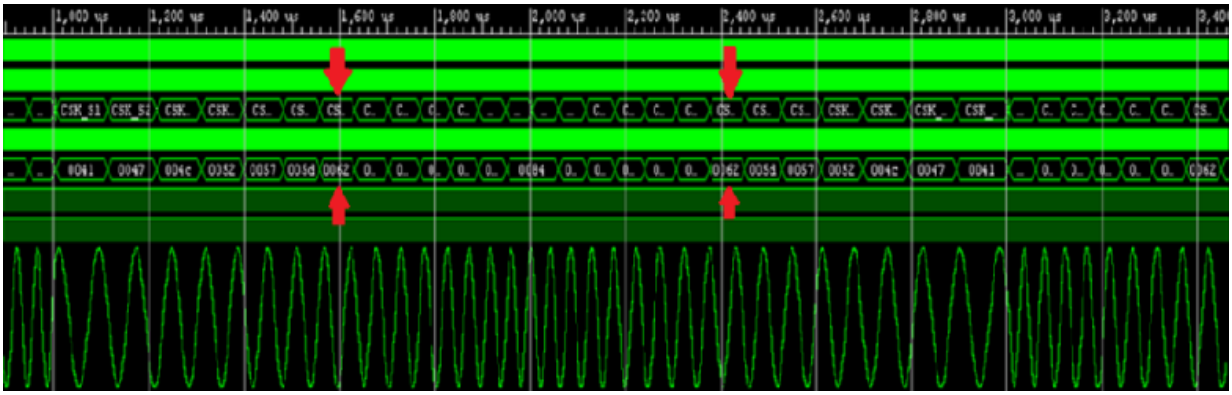

Fig.8: 24KHz Chirp signal reflected with "**x0084"** frequency word with amplitude- 1 V p-p and Time period t=0.0416 milliseconds**.**

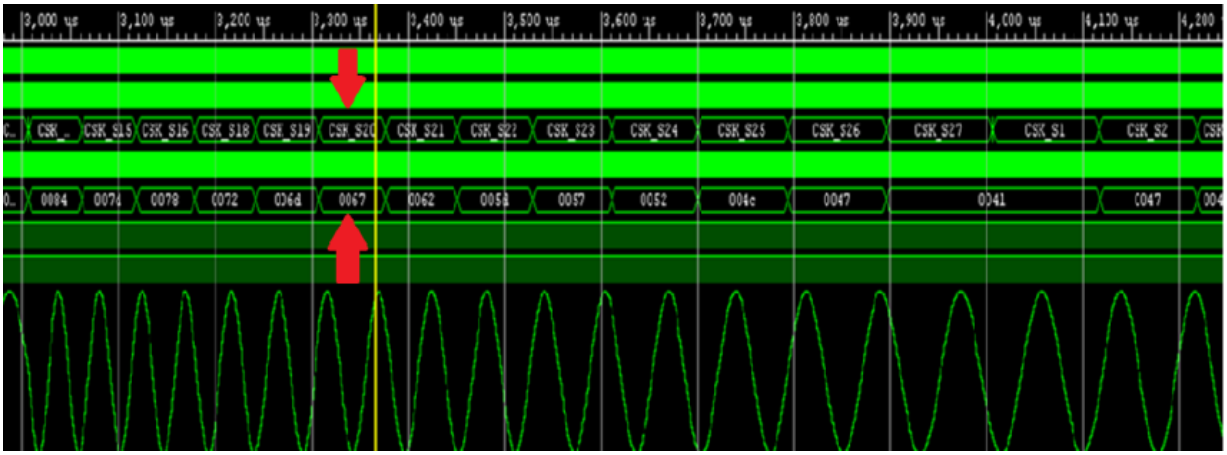

Fig.9: 18KHz Chirp signal reflected with "**x0062"** frequency word with amplitude- 1 V p-p and Time period t= 0.555 milliseconds.

2. Synthesis Reports of DDS-CSK Design

i) Device Utilization Summary

Figure.10 shows the complete components utilization summary of the DDS-CSK design.

```
Device utilization summary:
---------------------------

Selected Device : 7z030fbg676-3


Slice Logic Utilization:
 Number of Slice Registers:                26  out of  157200      0%
 Number of Slice LUTs:                    144  out of  78600       0%
    Number used as Logic:                 144  out of  78600       0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:      146
   Number with an unused Flip Flop:       120  out of     146     82%
   Number with an unused LUT:               2  out of     146      1%
   Number of fully used LUT-FF pairs:      24  out of     146     16%
   Number of unique control sets:           2

IO Utilization:
 Number of IOs:                           10
 Number of bonded IOBs:                   10  out of     250      4%
```

Fig.10: Design Components Utilization report.

ii) HDL Synthesis summary

Fig.11 shows the information regarding the confirmation report of HDL synthesis of DDS-CSK design.

```
                        HDL Synthesis
--------------------------------------------------------------------------
 States              | 31                                                 |
 Transitions         | 54                                                 |
 Inputs              | 14                                                 |
 Outputs             | 13                                                 |
 Clock               | CSK_CLK (rising_edge)                              |
 Power Up State      | csk_s0                                             |
 Encoding            | auto                                               |
 Implementation      | LUT                                                |
--------------------------------------------------------------------------

    Summary:
        inferred   1 Adder/Subtractor(s).
        inferred  32 D-type flip-flop(s).
        inferred  13 Comparator(s).
        inferred  37 Multiplexer(s).
        inferred   1 Finite State Machine(s).
Unit <CSK> synthesized.
```

Fig.11: HDL Synthesis Confirmation Report

iii) Clock Delay Analysis:

Following analysis shows the total time delay report of the entire design and it takes 3.181 ns.

```
Total                      3.181ns (0.533ns logic, 2.648ns route)
                                   (16.8% logic, 83.2% route)
```

iv) RTL Schematics:

The below figure Fig.12 shows the RTL schematic view of Chirp Slope Keying Modulation module.

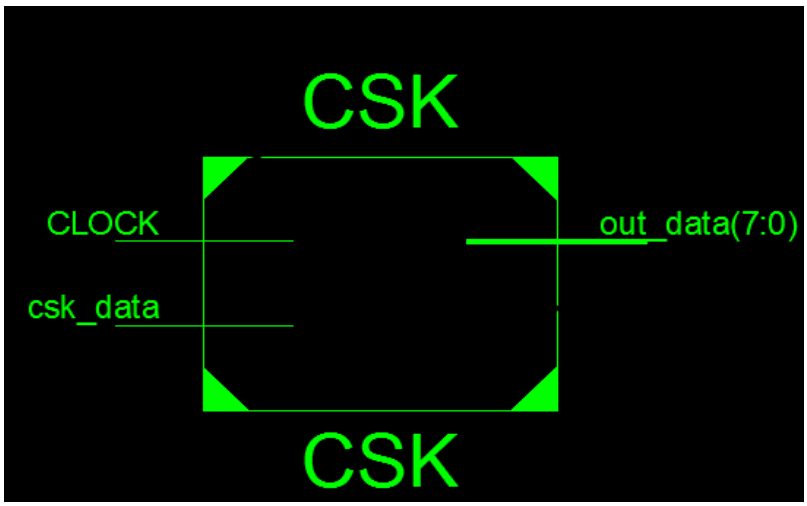

Fig.12: RTL view of Chirp Slope keying modulation design

The below figures Fig.13 and Fig.14 shows the actual RTL view of DDS signal generator component and entire design view.

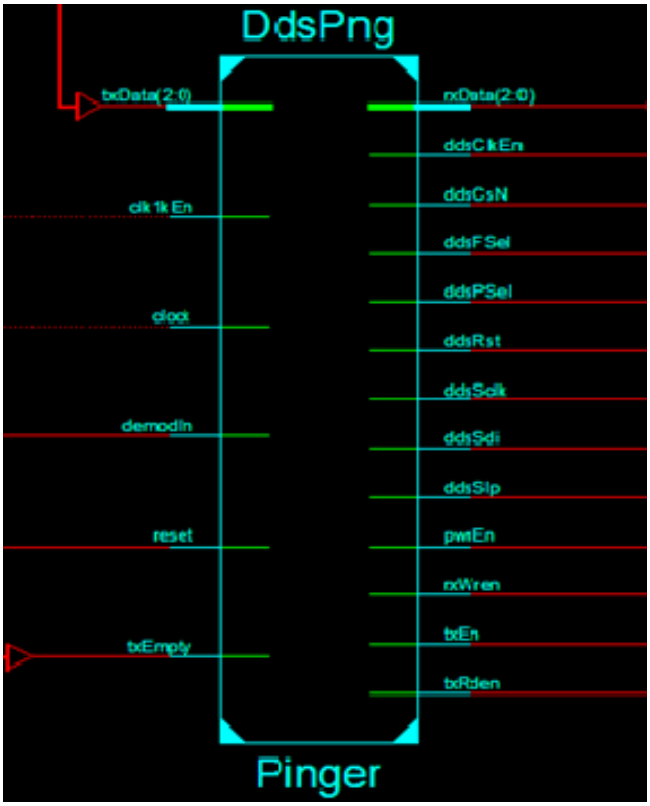

Fig.13: RTL view of AD9834 DDS component

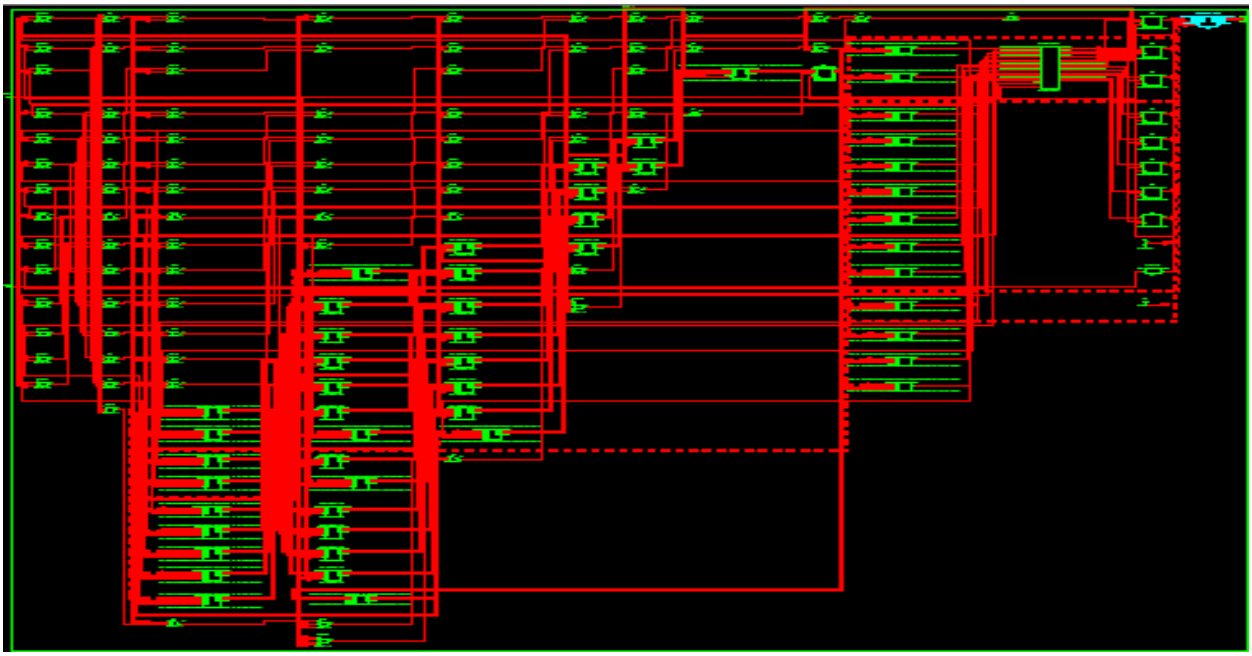

Fig.14: RTL view of entire Chirp Acoustic Modem design.

v) Design Power Analysis Report:

The below figure Fig.13 shows the total power consumption of DDS-CSK design on ZYNQ FPGA and it is observed that the total on chip power optimized is of 0.255W with a junction temperature of 25.5^{0}C.

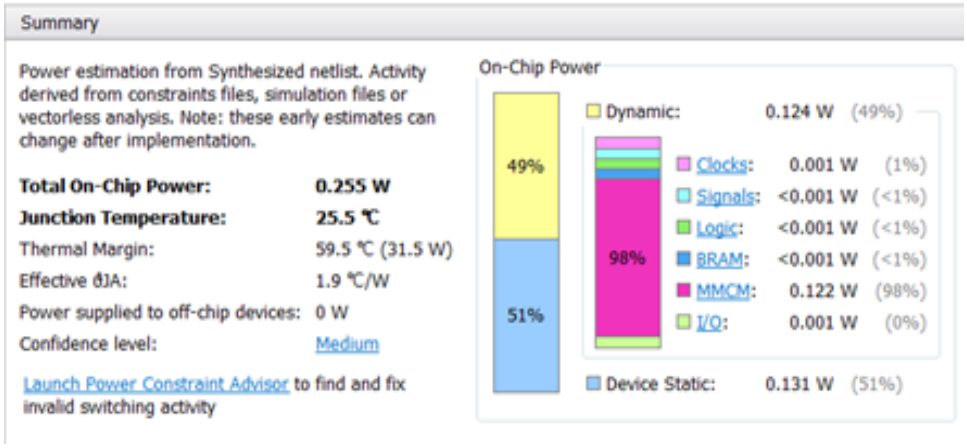

Fig.15: Power Consumption analysis of DDS-CSK design

vi) Design IP generation:

The entire design of DDS signal generator integrated with Chirp acoustic modem is further processed for IP (Intellectual Property) module where the entire design can be stored as a predefined building block. The above said can be generated by using VIVDADO IP generator tool which is provided in the software. The below figure Fig.16 is the final IP diagram of Chirp acoustic modem.

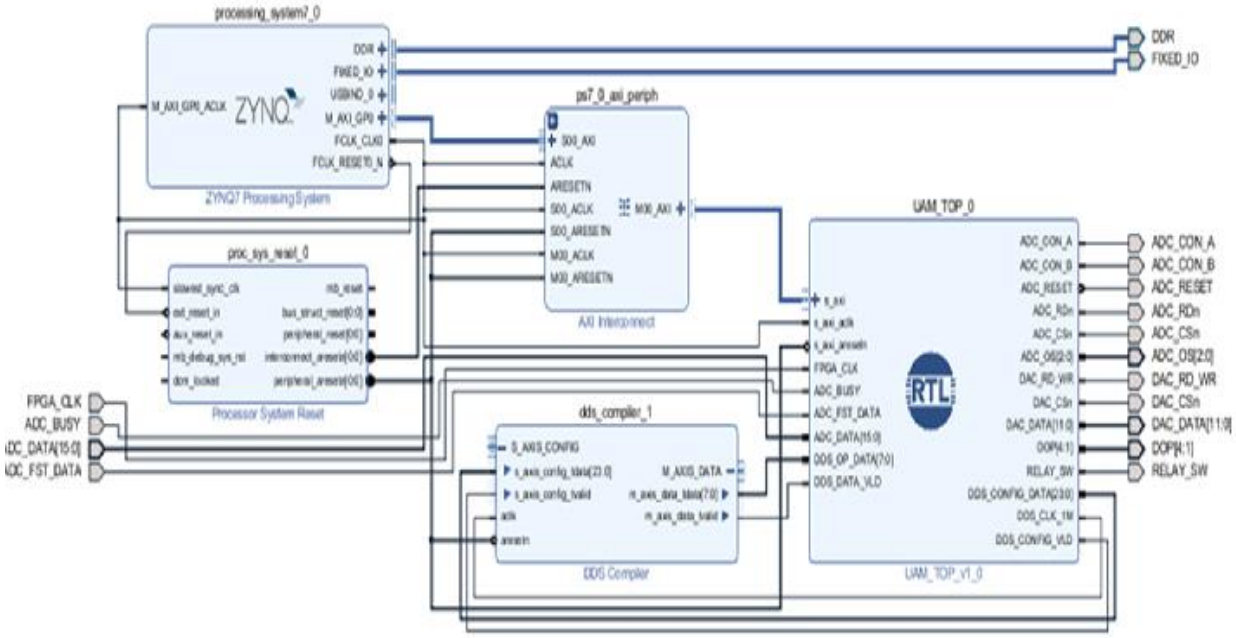

Fig.16: IP generation diagram of Chirp Acoustic Modem Design.

The above figure Fig.16, the ZYNQ interface module is interconnected with DDS module, peripheral interfacing module and Chirp Acoustic Modem module and as a whole stored as a unique IP.

vii) FPGA Board Results:

After verifying the simulations with possible test cases, the final code is implemented on the targeted FPGA hardware using Xilinx Vivado design flow, the bit file is dumped on to the board and the respected results (Fig.17 & Fig.18) are observed on the oscilloscope.

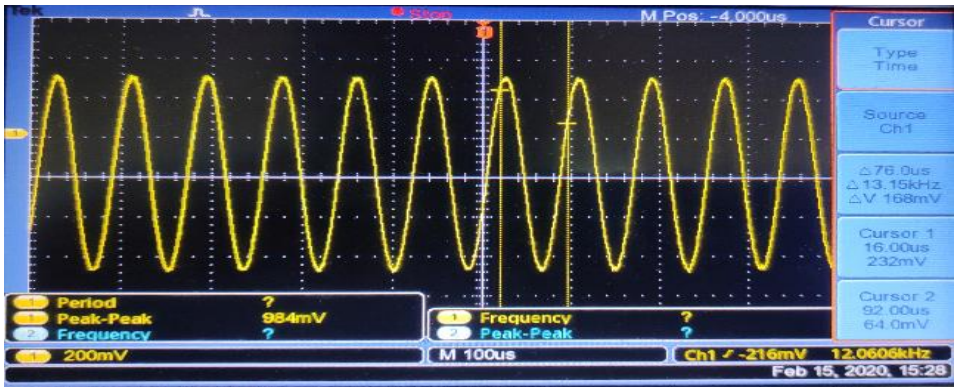

Fig.17: A 12 KHz Chip signal with time period t=0.083 milliseconds generated by DDS which is executed on Chirp Acoustic modem and observed in oscilloscope.

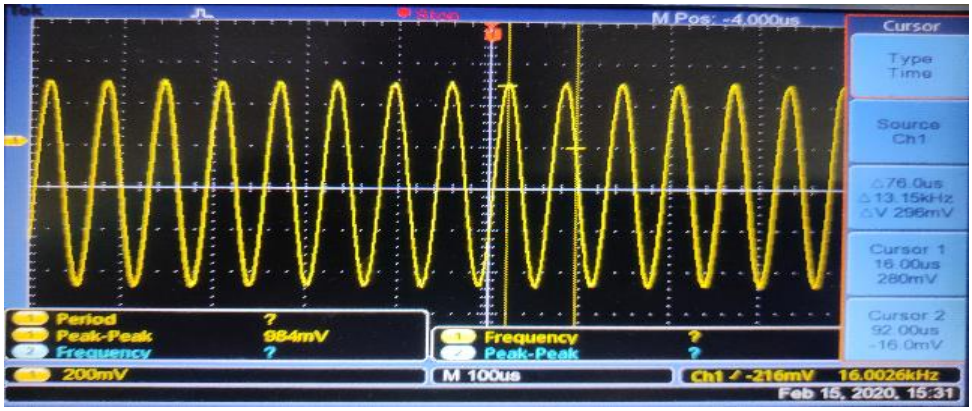

Fig.18: A 16 KHz Chip signal with time period t=0.062milli seconds generated by DDS which is executed on Chirp Acoustic modem and observed in oscilloscope.

VI. CONCLUSION

- Investigations on wireless acoustic communication and their communication setups conducted in this study. The generation of **Chirp / LFM** (Linear Frequency Modulated) signals using Direct Digital synthesizer (AD9834) signal generator is functionally simulated & observed.

- The architecture of ZYNQ FPGA based Chirp acoustic modem and the wireless communication transaction is explained in this paper.

- By using the hardware ZYNQ FPGA, and DDS signal generator, chirp signals ranging from 12KHz to 17KHz are generated by using DDS working principle and Chirp Slope Keing methology followed by FPGA implementation using Model based design tool.

- The DDS generated chirp signals (Fig 17, Fig 18) are shown in final results section. Further the design RTL schematics and Design IP schematic are extracted from the tool and established.

VI. ACKNOWLEDGEMENT

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